Serially-Connected Monolayer MoS_2 FETs with Channel Patterned by a 7.5 nm Resolution Directed Self-Assembly Lithography

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Abstract: We demonstrate sub-10 nm transistor channel lengths by directed self-assembly patterning of monolayer MoS_2 in a periodic chain of homojunction semiconducting-(2H) and metallic-phase (1T') MoS_2 regions with half-pitch of 7.5 nm. The MoS_2 composite transistor possesses an off-state current of 100 pA/μm and an I_{on}/I_{off} ratio in excess of 10^5. Modeling of the resulting current-voltage characteristics reveals that the 2H/1T' MoS_2 homojunction has a resistance of 75 Ω.μm while the 2H-MoS_2 exhibits low-field mobility of ~8 cm^2/V.s and carrier injection velocity of ~10^6 cm/s.

Introduction: 2D crystals of layered transition metal dichalcogenides (2D-TMDCs) such as MoS_2 are ideal candidates for aggressive miniaturization of field-effect transistors (FETs) to the single digit nanometer scale. In addition to large bandgap, chemical stability and compatibility with CMOS processes [1, 2], this class of materials can benefit from their atomically thin body with dangling-bond-free surfaces. Because of this and their ultra-small body thickness which leads to very small electrostatic characteristic scaling length, $\lambda=\sqrt{(\varepsilon_s.t_s.t_{ox}/\varepsilon_{ox})}$, transistor subthreshold swing (SS) and drain-induced barrier lowering (DIBL) coefficient in such films can be significantly smaller than for conventional thin-body semiconductors. In particular, monolayer-MoS_2 (ML-MoS_2), because of its bandgap of 1.8 eV yields high I_{on}/I_{off} ratio MOSFETs, while its low dielectric constant, ε_s = 4-7, and atomically thin body, $t_s \approx 0.7$ nm, facilitate the reduction of λ. In our previous work [3], we reported a 15-nm channel length MoS_2 FET using monolayer graphene as the Source/Drain (S/D) contacts. In this work, by exploiting the semiconducting to metallic phase transition in MoS_2 [4], we demonstrate a sub-10-nm transistor channel length by patterning of MoS_2 in a periodic chain of homojunction semiconducting- (2H) and metallic-phase (1T') MoS_2 regions. The 2H- to 1T'-phase transition occurs by exposing 2H-MoS_2 to *n*-butyl lithium solution as confirmed by electrical and photoluminescence measurements (Fig.1). Sub-10 nm 1T'/2H MoS_2 patterning is achieved by directed self-assembly (DSA) of block copolymers (BCP) technique which is one of the most promising emerging technologies for cost-effective, nanoscale, and high-volume manufacturing [5].

Device Fabrication: The key steps for fabricating BCP patterned MoS_2 FETs, as well as a schematic of the devices are shown in Figs. 2 and 3, respectively. ML-MoS_2, grown by chemical vapor deposition (CVD), was transferred onto a [p^+ Si/native SiO_2] substrate coated with 10 nm of HfO_2 (EOT≈ 4 nm) serving as the back gate (BG). Subsequently, by means of electron beam lithography and Au metallization, end-contacts to the MoS_2 film and measurement pads were formed. Next the surface of the substrate is functionalized with hydroxyl terminated polystyrene (OH-PS), poly(styrene-*b*-dimethylsiloxane) (PS-*b*-PDMS) BCP solution is spun-on followed by a solvent vapor annealing step to promote microphase separation, and finally selective reactive ion etching (RIE) of PS matrix is done in a controlled O_2 plasma leaving behind oxidized-PDMS (ox-PDMS) lines parallel to the Au lines. Fig.4a shows the final ox-PDMS lines with half-pitch of 7.5 nm formed between Au lines contacting the MoS_2 film. Next, the phase transition treatment of the ox-PDMS-patterned MoS_2 is applied to selectively convert the uncovered underlying 2H-MoS_2 to 1T'-MoS_2, while the ox-PDMS-covered regions remain semiconducting. These alternating 2H-MoS_2/1T'-MoS_2 areas correspond to semiconducting and metallic regions with same length, and form a chain of transistors in series as shown in Fig. 4b. The resulting transistor pitch is equal to the BCP period, 15 nm, with channel length of 7.5 nm. The minimum number of transistors-in-series thus formed between a pair of 120-nm-spaced Au electrodes was 8.

Results and discussion: Fig. 5a shows the I_d-V_g evolution at three fabrication stages of an eventual chain of eight ML-MoS_2 FETs with 15 nm pitch. As can be seen, the ML-MoS_2 survives the PS etching step and still shows high I_{on}/I_{off} modulation. However, current degradation of more than two orders of magnitude is observed as well as higher SS and shifted threshold voltage (V_t) compared with the as-fabricated MoS_2-FET. These changes are the consequences of the MoS_2 surface being affected by the plasma radicals. The unwanted degradation is nevertheless direct indication that the PS film is fully etched and the gaps between PDMS lines are fully opened. The last I_d-V_g curve in Fig. 5a shows the same device characteristics after phase-transition treatment. Fig 5b shows the final device at different V_d values highlighting the significant increase of I_{off} at V_d=1 V, which can be attributed to direct source-drain tunneling in the individual FETs. Fig. 6a shows the model fit to the data using the MIT Virtual Source model [6]. The transfer curve below threshold is determined by the MoS_2 threshold voltage (~ -1V), gate capacitance (for 4 nm EOT) and carrier velocity (8x10^5 cm/s). Near and above threshold (V_g>0 V), the contact resistance (~20 kΩ.μm) dominates over the channel resistance until the Schottky contact resistance between the Au metal and MoS_2 is sufficiently low (~1 kΩ.μm for V_g>2 V). In this regime (V_g>2V), the channel resistance dominates again and the transport is determined by carrier mobility ($\mu \approx 8$ cm^2/V.s) and series resistance between 1T'/2H MoS_2 homojunction (~ 75 Ω.μm). Fig. 6b shows the predicted transfer characteristics of an idealized single 7.5 nm MoS_2 transistor assuming MoS_2-metal contact resistance of 100 Ω.μm, and double gate with appropriate work-function and EOT of 0.5 nm leading to a drastically improved SS (62 mV/dec), low DIBL (~20 mV/V) and higher ON current. The carrier velocity and mobility found here from the modeling of the experimental devices are comparable to previously estimated values [7-9]. With the current CVD growth technique, the I_{on} is 0.1 mA/μm for I_{off}≈10 pA/μm at V_d=0.5 V (Fig. 6b). Further improvement of carrier velocity is possible with improved film-growth method to meet ITRS requirements for future nodes.

Conclusions: We have demonstrated the operation of MoS_2 FETs with the shortest and thinnest S/D channel, namely ~7.5 nm long and ~0.7 nm thick, reported to date. The transistor chain shows $I_{on}/I_{off} \approx 10^6$ with I_{off} ≈100 pA/μm. Further improvement of I_{on} current is possible by improved growth of MoS_2 and thus increased carrier velocity and mobility to meet the current requirement for high performance.

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References:

[1]B. Radisavljevic, *et al.*, Nat. Nano. Vol. 6, no. 3, p 147, 2011
[2]W. Cao *et al.*, IEDM 2014.
[3] A. Nourbakhsh *et al.*, VLSI 2015.
[4] R. Kappera *et al.*, Nat. Mat. Vol. 13, p 1128, 2014
[5] S. Jeong *et al.* Mater Today 16, 468-476, 2013.
[6] A. Khakifirooz *et al.*, IEEE T Electron Dev. 56, 1674, 2009.
[7] W.Cao *et al.*, IEEE T Electron Dev. 2014.
[8] M. Luisier *et al.*, IEDM 2014.
[9] G. Fiori *et al.*, APL 2013

MoS_2 FET fabrication

(a) 90 nm SiO_2/p^{++} Si wafer
(b) (i) SiO_2 wet etch by BOE, (ii) ALD HfO_2, (iii) forming gas anneal
(c) Transfer MoS_2 films from growth substrates onto target substrates
(d) Au end-contacts and measurement pad metallization

DSA-BCP patterning and phase transition treatment

(e) Apply hydroxyl terminated PS to the substrate
(f) Spin coat PS-*b*-PDMS BCPs blend on the substrate
(g) Solvent vapor anneal using toluene and acetone vapor
(h) CF_4 RIE etch to remove the top PDMS wetting layer
(i) O_2 RIE etch to remove PS matrix
(j) Immerse PDMS-patterned MoS_2 FET in 2% *n*-butyl lithium
(k) *n*-butyl lithium removal by solvent rinse

Fig. 2. Fabrication process flow of the short channel 1T'/2H MoS_2 FETs patterned by DSA-BCP technique. Step (b) includes ALD-HfO_2 at 200 °C, followed by annealing in a forming gas at 400 °C.

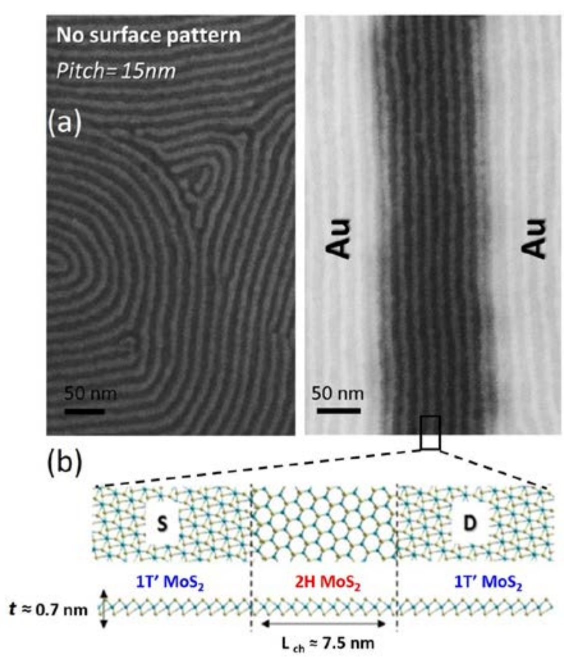

Fig.4. (a) SEM images show ox-PDMS lines with 15 nm pitch after PS etch on surfaces with no guide pattern as well as surfaces with Au lines as directional guides. The absence of pattern leads to random formations of the ox-PDMS lines while in patterned surface lines are self-assembled in parallel with the Au electrodes. (b) Schematic short channel FET comprised of a 2H-MoS_2 channel contacted to two adjacent metallic 1T'-MoS_2 regions forming S/D contacts.

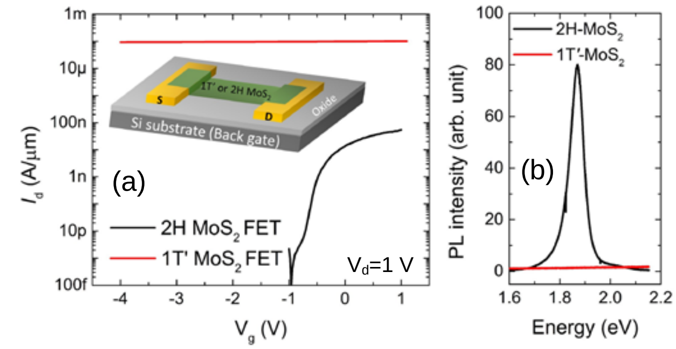

Fig. 1. (a) I_d-V_g of a long-channel MoS_2 FET before and after phase transition treatment. The intrinsic 2H-MoS_2 FET shows strong semiconducting behavior with large gate modulation, while after the phase transition, it shows constant (compliance) current due to metallic 1T'-MoS_2. (b) PL spectra of monolayer 2H- and 1T'-MoS_2: The 2H phase shows a strong PL peak at 1.85 eV, while the PL of the 1T'-phase is absolutely quenched owing to its gapless metallic characteristics.

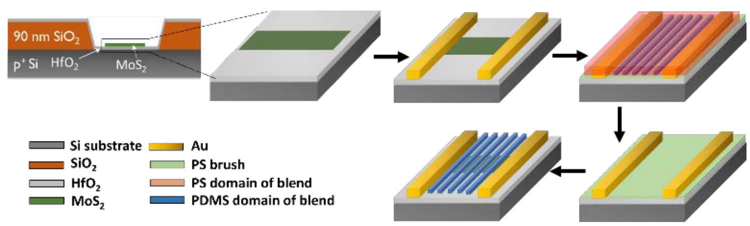

Fig. 3. Schematics depicting the different steps of the DSA of BCP on MoS_2 FETs

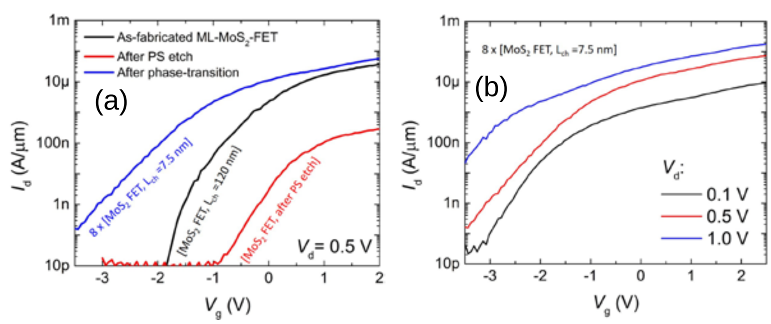

Fig. 5. (a) Evolutions of I_d-V_g at V_d = 0.5 V of a CVD monolayer MoS_2-FET: As-fabricated (black), after PS etch (red) and final (blue) after phase transition treatment with *n*-butyl lithium. (b) I_d-V_g of the final device (8x MoS_2 FETs, L_{ch}=7.5nm) at different V_d values.

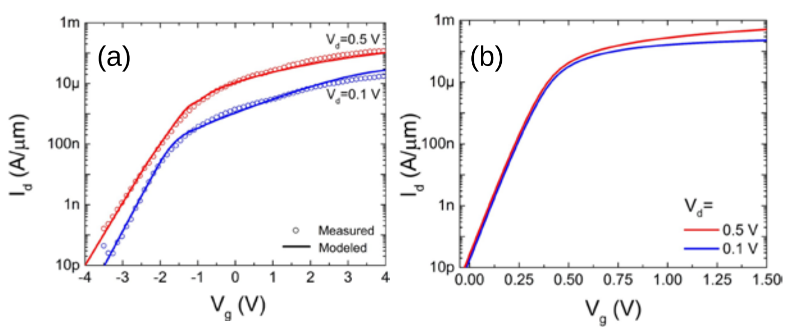

Fig. 6. (a) MVS fit of the experimental data for the 8 transistor array, high end-contact resistance dominates transport above threshold and limits the I_{on} below 100 µA/µm. (b) Performance prediction of a single transistor with a double-gate structure, EOT of 0.5 nm, and with the same device parameters but assuming excellent contact resistance (100 Ω.µm). Threshold voltage is adjusted to +0.5V for this plot.