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Transport Properties of a MoS_2/WSe_2 Heterojunction Transistor and Its Potential for Application

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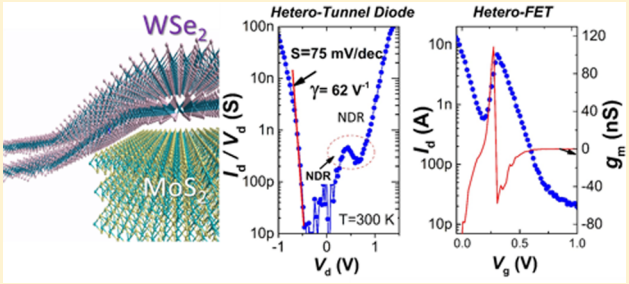
Supporting Information

ABSTRACT: This paper studies band-to-band tunneling in the transverse and lateral directions of van der Waals MoS_2/WSe_2 heterojunctions. We observe room-temperature negative differential resistance (NDR) in a heterojunction diode comprised of few-layer WSe_2 stacked on multilayer MoS_2. The presence of NDR is attributed to the lateral band-to-band tunneling at the edge of the MoS_2/WSe_2 heterojunction. The backward tunneling diode shows an average conductance slope of 75 mV/dec with a high curvature coefficient of 62 V^{-1}. Associated with the tunnel-diode characteristics, a positive-to-negative transconductance in the MoS_2/WSe_2 heterojunction transistors is observed. The transition is induced by strong interlayer coupling between the films, which results in charge density and energy-band modulation. The sign change in transconductance is particularly useful for multivalued logic (MVL) circuits, and we therefore propose and demonstrate for the first time an MVL-inverter that shows three levels of logic using one pair of p-type transistors.



KEYWORDS: *Transition metal dichalcogenide, heterojunction transistor, band-to-band tunneling, negative differential resistance, multivalued logic*

Two-dimensional (2D) crystals based on atomically thin-films of layered semiconductors, such as the family of transition metal dichalcogenides (TMDCs), offer an attractive platform for various optoelectronic applications[1−14] that stems from their unique electrical, mechanical, and optical properties. The 2D crystals derived from layered crystals, such as graphene, molybdenum disulfide (MoS_2), and hexagonal boron nitride (h-BN), have no dangling bonds on their surfaces. This is in distinct contrast to their counterpart quasi low-dimensional semiconductors, which are produced by thinning down conventional 3D crystals. The trapping sites induced by the dangling bonds in 3D crystal-derived quasi low-dimensional semiconductors are considered to be a major problem as they become trap and recombination sites. The 2D electronics can take advantage of the absence of dangling bonds to provide high quality electronic devices on an atomic scale.

The unique optoelectronic and crystal properties of atomically thin 2D crystals make them particularly attractive for heterojunction devices, which can potentially overcome some of the problems that conventional heterostructure devices face and thin 2D crystals also demonstrate novel photovoltaics and optoelectronic applications. Lee et al.[8] reported an atomically thin p−n vertical junction consisting of van der Waals-bonded monolayers of MoS_2 and WSe_2. The junction shows strong rectifying electrical characteristics and photovoltaic response. Additionally, Fang et al.[15] demonstrated evidence of strong electronic coupling between the 2D MoS_2 and WSe_2 layers, which leads to a new photoluminescence (PL) mode in this artificial van der Waals heterostructure.

A very promising field of applications for van der Waals heterostructures of 2D crystals is as interband tunneling transistors for low power applications. Such van der Waals heterostructures can in principle benefit from atomically sharp interfaces. This is crucial for tunneling devices that suffer from impurities and interfacial defects. Moreover, the wide range of available 2D crystals allow different band-edge alignments with distinct band energy structures, ranging from the gapless graphene with a symmetric electron and hole band structure to the wide band gap semiconductors and insulators.

Several in-plane tunneling transistors based on 2D and 1D semiconductors, such as carbon nanotubes,[16] bilayer graphene,[17] graphene nanoribbons,[18] and so forth, have been studied. However, interlayer tunneling devices, which require tunneling in the vertical direction of 2D crystals, are still in their early stages and need further in-depth studies to obtain band structure parameters and tunneling probability along their out-of-plane direction to assess their suitability for high performance tunneling transistors. Nevertheless, some vertical field-effect transistors (FETs) comprising stacks of 2D crystals have already been reported. Britnell et al.[19] and Kang et al.[20]

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demonstrated graphene/h-BN/graphene vertical tunneling transistors with h-BN as the tunneling barrier. This device shows quantum electron tunneling through the barrier modulated by electrostatic gating of the graphene layers.

Recently, Yan et al.[21] demonstrated an Esaki diode based on a heterojunction composed of a van der Waals stack of $SnSe_2$ and black phosphorus crystals separated by a native thin tunneling barrier. Their diode showed strong negative differential resistance (NDR), which confirms band-to-band tunneling in this van der Waals heterojunction. However, black phosphorus is unstable when exposed to ambient conditions and rapidly degrades.[22] As mentioned above, 2D crystals that have stable chemical structures, such as MoS_2 and WSe_2, are very promising for creating ultraclean, defect-free heterointerfaces. In a pioneering work, Roy et al.[23] reported evidence of band-to-band tunneling in a MoS_2/WSe_2 diode. Esaki diode characteristics were observed with NDR at temperatures below 125 K. The authors speculate that band-to-band tunneling occurs in the vertical direction.

The present work aims to provide further understanding of the transport properties in MoS_2/WSe_2 heterojunction FETs (hetero-FET). Despite the earlier work on the optoelectronic properties of MoS_2/WSe_2 devices, the transfer characteristic features of such devices are yet to be fully discussed in the literature. The first part of this work studies a novel feature in the transfer characteristics (I_d–V_g) and transconductance (g_m) of a generic MoS_2/WSe_2 hetero-FET. We present an optimized device geometry to enhance the transfer characteristic parameters to be suitable for high performance electronics. We then discuss the possibility of band-to-band tunneling in this heterojunction. We answer the question whether the vertical (or out-of-plane) direction is the dominant path for band-to-band tunneling in the MoS_2/WSe_2 heterojunction by simulating and comparing the band diagrams of the heterojunction in both the in-plane and out-of-plane directions. We also design a MoS_2/WSe_2 tunnel diode based on the information obtained from the simulation and we investigate its tunnel diode characteristics. Finally, a novel application of the optimized MoS_2/WSe_2 hetero-FET as a building block for multivalued logic is provided.

Figure 1a shows the transfer characteristics (I_d–V_g) of generic few-layer (2–4 layers, confirmed by atomic force microscopy (AFM)) MoS_2- and WSe_2-FETs, where V_g is the voltage applied to the substrate. The MoS_2 FET, consistent with previous literature, is shown to be an n-type semiconductor, while WSe_2 demonstrates both n- and p-type characteristics giving rise to ambipolar transfer characteristics with a relatively wide OFF-state region. The symmetry of the electron and hole conductions of the WSe_2 FETs can be strongly affected by the Schottky barrier at the WSe_2–metal junction. High-performance ambipolar WSe_2-FETs have already been reported using dissimilar low and high work function metal contacts to obtain low-resistance, ohmic contacts to electrons and holes, respectively.[7,24]

Figure 1b plots the transfer characteristics of a MoS_2/WSe_2 hetero-FET arranged in the in-series mode. In this configuration, the MoS_2 and WSe_2 films form an overlapped region so that the source and drain electrodes (S/D) are in contact with the films, while leaving the overlapped region away from direct contact with the electrodes. In this configuration, electrons injected from the source to the MoS_2 film have to proceed through the WSe_2 film in the overlapped region and continue to the drain electrode. Therefore, the MoS_2 and WSe_2 films can

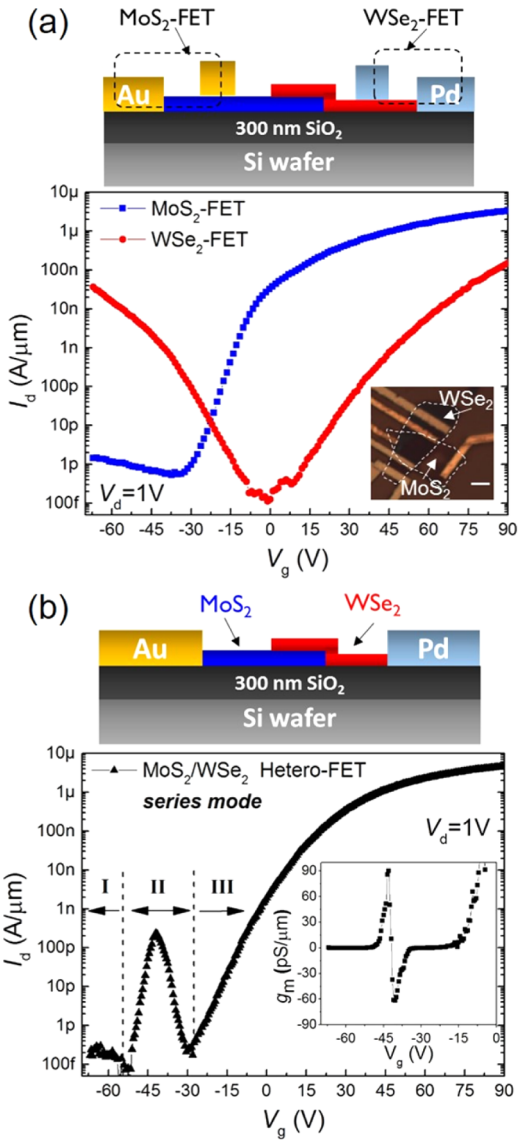

Figure 1. (a) Transfer characteristics (I_d–V_g) of a back-gated few-layer MoS_2- and WSe_2-FET. The inset shows an optical image of a typically stacked MoS_2/WSe_2 FET. The scale bar is 5 μm. (b) I_d–V_g of the MoS_2/WSe_2 heterojunction FET in the series measurement mode. The inset shows the transconductance centered around the peak in region II. The schematics show the corresponding device measurement setups.

independently modulate the overall transport characteristics of the FET. As shown in Figure 1b, I_d–V_g of a back-gated in-series MoS_2/WSe_2 FET shows three distinct regions. In region I (V_g < −53 V), I_d is very low within the noise of the measurement setup. This region is modeled by an i–p^+ junction because the MoS_2 is depleted, while the WSe_2 shows hole accumulation. Therefore, the electron path from source to drain is blocked by highly resistive depleted MoS_2, which results in low current. However, in region II (−53 V < V_g < −30 V), the current increases and shows a peak with substantial current centered at −42 V with a peak-to-valley ratio in excess of 1000. This region corresponds to the condition where the MoS_2- and WSe_2-FET are both in their subthreshold regimes, where decreasing V_G from −30 to −53 V leads to an exponential increase of hole conduction on the WSe_2 side and an exponential decrease of the electron concentration on the MoS_2 side toward its

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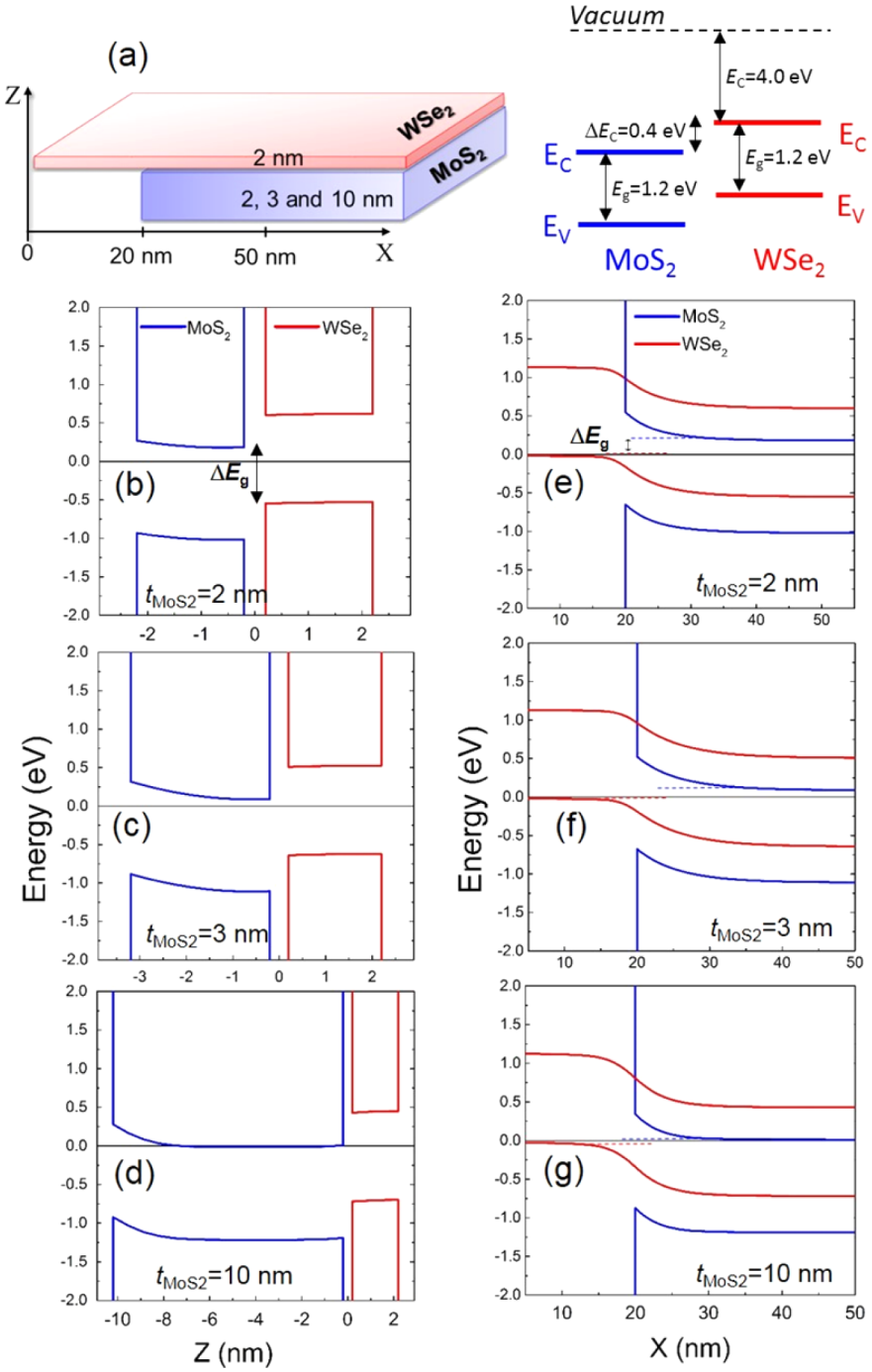

Figure 2. (a) Schematic of a MoS_2/WSe_2 heterostructure and the conduction band (E_C) and valence band (E_V) positions that are used for calculation of the band diagrams. (b–d) Calculated band diagrams of MoS_2/WSe_2 heterojunctions in the out-of-plane direction at the middle of the overlapped region (X = 50 nm). The WSe_2 is 2 nm thick while the thickness of MoS_2 varies as (b) 2, (c) 3 and (d) 10 nm. (e–g) In-plane band diagram of the same heterojunctions along the X-axis of the schematic in (a) at edges of the MoS_2 and WSe_2 films. In all the structures, the WSe_2 charge is $5 \times 10^{18}/cm^3$ and the MoS_2 charge density is $1 \times 10^{19}/cm^3$, which are in the typical range that can be achieved by both chemical and electrostatic doping and the gap between the MoS_2 and WSe_2 films is 4 Å, assuming that there is a van der Waals gap between the two films. See Figure S7 of the Supporting Information for the band diagrams of 2 nm WSe_2/10 nm MoS_2 with different charge densities.

depletion regime. Hence, this condition can be assigned to a $p^-–n^-$ junction. The resulting current peak shows a rapid change in the gated transconductance ($g_m = dI_d/dV_g$) from positive to negative, as shown in the inset of Figure 1b. This feature, which occurs when one of the semiconductor layers (MoS_2 here) is near its depletion condition, is distinct from the negative transconductance owing to the resonance tunneling phenomena, which occurs at matched carrier densities in two-dimensional electron gas systems (2DEGs).[25−28] We will then further discuss this sign-changing g_m characteristic and its possible application.

At larger V_g, region III, the current increases monotonically with increasing V_g. The current in this region is dominated by electron conduction in both the MoS_2 and WSe_2 regions, as both are in their electron accumulation regimes. Therefore, for this region, the system can be modeled by an n–n

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heterostructure. Figures S3 and S6 in the Supporting Information show the photoresponse of the in-series MoS_2/WSe_2 FET and transfer characteristics of a MoS_2/WSe_2-FET in the parallel mode, respectively.

Similar to 2DEG bilayer heterostructures,[17,29] the most interesting transport regime in the MoS_2/WSe_2 FET shown in this work is when the MoS_2 and WSe_2 layers are oppositely charged and form a p−n heterojunction. Heterostructure semiconductors are widely used for the fabrication of tunneling FETs (TFETs), which are among the most promising devices for achieving very low power operation, owing to the possibility of achieving a steep inverse subthreshold slope below the thermionic limit of 60 mV/decade. In principle, heterojunction TFETs, using two different semiconductors forming a vertical or horizontal junction, are interesting compared with homojunction TFETs, as they enable bandgap engineering to form a heterojunction with a narrower effective bandgap, which improves the tunneling probability and, thus, the drive−current that significantly depends on the bandgap. A variety of semiconductor heterostructures, especially those based on III−V compounds, have already been fabricated to make heterojunctions with the desired bandgap features. Examples include GaAsSb/InGaAs,[30,31] InP/InGaAs,[32] and GaSb/InAS.[33] Analogous to these conventional bilayer heterojunctions, bilayer heterojunctions of van der Waals stacked 2D materials, such as the ones studied in this work, are considered very promising for tunneling devices. As was mentioned earlier, the charge transferred between the layers can strongly modulate the energy bands of WSe_2 and MoS_2 forming a region with an abrupt, atomically precise interface that is of high importance, as nonidealities, such as defects and nonabrupt band-edges, owing to, for example, the random doping distribution case, are critical in TFET technology.

To determine the possible band-to-band tunneling paths in a MoS_2/WSe_2 heterojunction, we calculated the band diagram of some representative MoS_2/WSe_2 heterojunctions with different charge densities and film thicknesses. The details of the calculations can be found in the Supporting Information. Figure 2b−g shows band diagrams of the heterojunction between a 2 nm thick p-doped WSe_2 (equivalent to a three-layer WSe_2) with charge density of $5 \times 10^{18}/cm^3$ and an n-doped MoS_2 with bulk charge density of $1 \times 10^{19}/cm^3$ for three different thicknesses, (i) t_{MoS2} = 2 nm, t_{WSe2} = 2 nm, (ii) t_{MoS2} = 3 nm, t_{WSe2} = 2 nm, and (iii) t_{MoS2} = 10 nm, t_{WSe2} = 2 nm (Figure 2a shows a schematic of the MoS_2/WSe_2 layers and the conduction band and valence band alignments used for calculation of the band diagrams). The band diagram in the transverse direction (i.e., Z) (Figure 2b−d) of the heterojunction interface shows a minimum effective band gap of ΔE_g = 0.85 eV between the conduction band of WSe_2, $E_{C,WSe2}$ and the valence band of MoS_2, $E_{V,MoS2}$, which corresponds to t_{MoS2} = 10 nm, t_{WSe2} = 2 nm. This is a relatively large band gap for a tunneling device compared with other proposed heterostructures that have been developed for high-performance TFETs, because the tunneling probability decreases as the effective band gap increases. In addition, the weak van der Waals interaction between the layers, owing to the random orientation of their lattices, leads to an effective vacuum potential barrier. This further suppresses the tunneling probability and therefore the tunneling current. Therefore, vertical tunneling in MoS_2/WSe_2 seems very unlikely. However, the band diagram along the horizontal direction (i.e., X), plotted in Figure 2e−g shows promising features. In fact, owing to the thin nature of the films, the interaction between layers at the junction leads to substantial band bending between the overlapped and nonoverlapped regions. As expected, the band bending is stronger in the thinner film and the effective band gap ΔE_g strongly decreases with increasing the asymmetry of the thicknesses of the layers. In the case of 2 nm WSe_2/10 nm MoS_2, a small in-plane ΔE_g < 50 meV is achieved, compared with 0.85 eV in the transverse band diagram at the overlapped region. The band diagram of the 2 nm WSe_2/10 nm MoS_2 heterojunction predicts the occurrence of NDR owing to band-to-band tunneling between the conduction band (E_C) of MoS_2 in the overlapped region and the valence band (E_V) of WSe_2 of the nonoverlapped region.

Before discussing the experimental results of the predicted tunneling performance, we would like to highlight once again that in modeling 2D materials-based heterojunctions in addition to the band alignment in the transverse direction the band structure modulation along the interface needs to be taken into account to obtain a comprehensive evaluation of the transport in any ultrathin low or moderately doped heterostructure device. This also enables the selection of suitable materials for NDR enhancement. Additionally, despite the promising features of van der Waals TMDC heterostructures the out-of-plane carriers possess heavier masses in the layered materials than the masses parallel to the layers (e.g., MoS_2, in-plane mass = 0.45 m_e, out-of-plane mass =1.73 m_e[34]). Additionally, the out-of-plane resistance can be orders of magnitude larger than the in-plane resistance, which is a consequence of their anisotropic nature owing to the weak van de Waals interlayer interaction compared with the strong covalent in-plane interaction between atoms. However, a comprehensive, quantitative study is required to obtain an in-depth understanding of tunneling transport in both the in-plane and out-of-plane directions in 2D heterojunctions. Nevertheless, knowing that in general the tunneling transmission probability[17,35] is $T(F) = \exp\left(\frac{-\pi(m^*_{tunnel})^{1/2}\Delta E_g^{3/2}}{2\sqrt{2}\hbar qF}\right)$ (where m^*_{tunnel} is the carrier effective mass in the tunneling direction, ΔE_g is the effective bandgap, and F is the electric field across the semiconductor body), we can anticipate that the heavier carriers in the out-of-plane direction as well as the larger band gap can dramatically decrease the tunneling probability in this direction compared with the in-plane direction. Hence, given the smaller in-plane carrier masses and band gap, the in-plane heterojunction of TMDC atomic layers, as discussed above, promises to be a practical structure for actual tunneling devices. However, one should consider that in such van der Waals heterojunctions, carriers in both horizontal and vertical directions still have to tunnel through an extra effective van der Waals barrier. However, this barrier, which can be considered as a square barrier, is thinner (<1 nm) than the tunneling distance. Therefore, the tunneling barrier height defined by the effective bandgap, remains the main crucial tunneling parameter.

Next, to evaluate the possibility of band-to-band tunneling in an in-plane MoS_2/WSe_2 heterojunction, as suggested by the afore-discussed band diagram, we study a transistor whose channel comprises of a thickness-asymmetric ∼2 nm WSe_2/∼10 nm MoS_2 stack (thicknesses confirmed by AFM measurements). For a comparison of I_d−V_d of MoS_2/WSe_2 stacks with different thicknesses, see the Supporting Information. To enhance the performance of the transistors and

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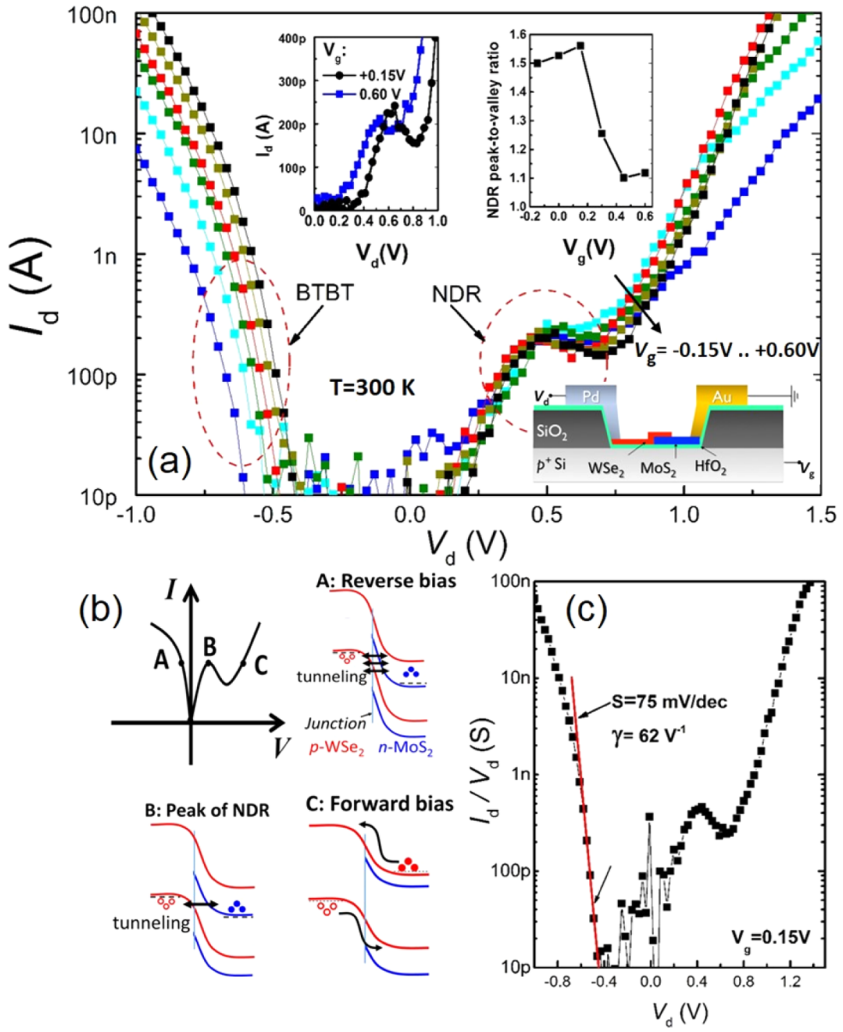

Figure 3. (a) Room temperature I_d–V_d of a 10 nm MoS_2/2 nm WSe_2 transistor at different V_g values. The insets show I_d–V_d at the NDR region with a linear scale for V_g = +0.15 V (black) and +0.60 V (blue) on the left and NDR peak-to-valley ratio versus V_g on the right. The schematic shows the corresponding device measurement setups. (b) Schematic band diagrams of a MoS_2/WSe_2 junction at points A, B, and C, illustrating the three different bias regimes. (c) Conductance ($G = I_d/V_d$) versus V_d at V_g = 0.15 V.

improve the gate efficiency, we need to increase the gate dielectric capacitance and yet keep the gate leakage current as low as possible. Herein, we fabricate the transistor channel on a thin high-k dielectric, for example, HfO_2, while the metal pads and wires are isolated using a thick SiO_2 layer to optimize the trade-off between the gate efficiency and gate-source/drain leakage current. The details of the device fabrication process can be found in the Supporting Information.

Figure 3a shows the room temperature I_d–V_d in reverse and forward bias regions at different V_g values. In the forward bias region, a clear NDR with a maximum peak to valley of 1.6 is observed at V_g = 0.15 V. The insets show the NDR region in the linear scale for V_g = 0.15 and 0.60 V and the NDR peak to valley ratio versus V_g, which decreases monotonically by increasing V_g to 0.60 V. In fact, applying a more positive V_g widens the gap, owing to the different gate efficiencies associates with MoS_2 and WSe_2, which move the bands at different rates. This makes the NDR process more difficult and explains the decrease of the peak-to-valley values toward zero. Schematic band diagrams of the in-plane MoS_2/WSe_2 junction at different bias regimes are shown in Figure 3b.

Figure 3c shows the conductance ($G = \frac{I}{V}$) for V_g = 0.15 V. Our gated tunneling diode in the reverse bias regime shows an average conductance slope of S = 75 mV/dec over 2 orders of magnitude, and a maximum curvature coefficient ($\gamma = \frac{d^2I}{dV^2}/\frac{dI}{dV}$) of 62.2 V^{-1} above the noise level, at V_d = −0.45 V.

The curvature coefficient is an important figure of merit parameter for designing high-performance tunneling diodes that are promising devices for several applications, such as high-frequency detectors.[36] Because the operation of these diodes is based on band-to-band tunneling, their I–V curvature characteristics are not limited by their thermionic emission of carriers. Our tunnel diode reached the typical goal of γ > 40 V^{-1} for backward diode operation.[36] The best γ reported so far, based on Si and III–V semiconductor-based backward diodes, are in the range of 47 to 70 V^{-1} in the low V_d regime,[37−39] which places our MoS_2/WSe_2 tunnel diode among the highest performance tunnel diodes reported to date. However, to obtain a transistor with a subthreshold slope SS < 60 mV/dec, γ should be larger than 80 V^{-1}.[36] Given the fact that unlike the conventional semiconductor devices, where the charge concentration of the semiconductor is well-controlled by

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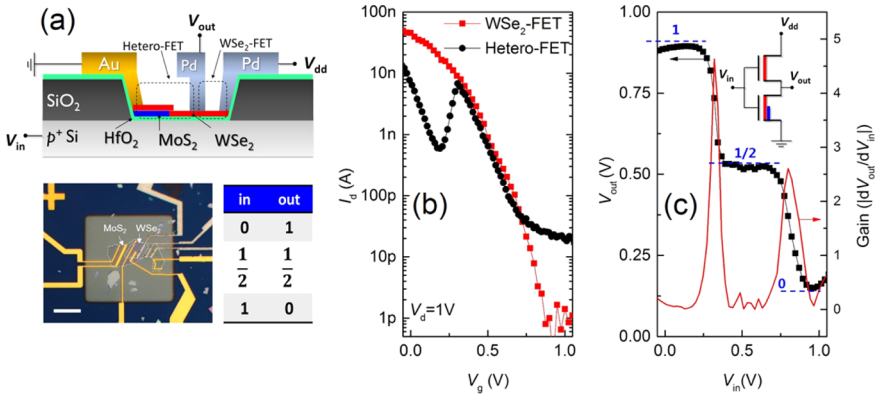

Figure 4. (a) Schematic of the ternary inverter, an optical image of the device, and an input−output table of the inverter. (b) Comparison of I_d−V_g curves of the hetero-FET and WSe_2-FET shown in (a). (c) V_{out} versus V_{in} plot of the ternary inverter showing three distinct levels of logic. The inset shows a circuit schematic of the inverter.

doping techniques, in this MoS_2/WSe_2 device, its unintentional, natural doping is not prepared through any specific doping approach. Developing efficient doping approaches to precisely control the charge density in 2D crystals and yet preserve their excellent properties will certainly aid in the preparation of the sharp band-edge feature in the 2D heterojunctions that is needed to observe the sharp threshold characteristics beyond the SS = 60 mV/dec limit.

Negative transconductance has been demonstrated in gated resonant tunneling devices[25] as well as modulation doped FETs.[27] Among different applications of negative transconductance, multivalued logic (MVL)[26] has attracted much attention. Owing to a higher number of logic states, MVL has the potential for higher data storage in less area as compared with binary logic.

In the past decades, MVL, such as ternary (three-level logic), has been considered as an alternative to binary logic and, so far, significant development has been achieved in the theory and design of ternary-based arithmetic operations.[40] Different MVL architectures, such as current-mode[41] and voltage-mode[42] multivalued CMOS, as well as multivalued charge-coupled devices[43] have already been demonstrated.

Herein, we demonstrate the application of MoS_2/WSe_2 heterojunction FETs with the sign-changing transconductance feature for a ternary inverter using only one type of FET (p-FET). The inverter, as schematically depicted in Figure 4a, comprises two FETs built on a WSe_2 film partially stacked on a MoS_2 film. The WSe_2 end is contacted by Pd and the overlapping region is contacted with Au. This configuration can be considered as a WSe_2-FET in series with a parallel-mode MoS_2/WSe_2 FET. For this device, an asymmetrical stack of a few-layer WSe_2 and a multilayer MoS_2 were used. The work function difference of MoS_2 and WSe_2[44] leads to charge accumulation of electrons in MoS_2 and of holes in WSe_2. Given the thin body of the WSe_2, this charge transfer creates two distinct regions in WSe_2: a part that overlaps with the MoS_2 and a nonoverlapped region that can be considered as p^+−p^- regions. This multicharge density profile induces multithreshold voltages (multi-V_{th}) in the transfer characteristics of a FET comprising the p^+−p^- regions. Figure 4b compares the I_d−V_g curves of the WSe_2-FET built on the overlapped region with the curve of the combined WSe_2 and overlapping WSe_2/MoS_2 (p^+−p^- channel), which is analogous with the FETs in Figure 1, and that we named a parallel-series mode FET. In region I of the I_d−V_g curves, which corresponds to the threshold regime, a strong decrease of the current, which gives rise to the negative transconductance feature, is observed. As a result, the current of the parallel-series FET in this region is lower than its WSe_2 counterpart FET, which shows regular I_d−V_g behavior. In region II, corresponding to the subthreshold region of both FETs, both devices behave similarly with parallel I_d−V_g curves. However, in region III or the OFF-state region, the WSe_2-FET has substantially lower current than the parallel-series FET owing to the fact that the OFF current of the parallel-series FET is larger. In the inverter configuration (inset of Figure 4c), the back gate is used for the input voltage (V_{in}), the middle electrode for output voltage (V_{out}), and the sides electrodes for the source and supply voltage. The three regions described in Figure 4b, form three distinct levels in the input−output characteristics (V_{out} versus V_{in}) of the inverter, shown in Figure 4c, corresponding to three logic states. In this plot, V_{in} varies in the range of 0−1 V where V_{out} shows a high value of ∼0.9 V for $0 < V_{in} < 0.3$ V, corresponding to state 1, a medium value of $V_{out} \sim 0.5$ V for $0.4 < V_{in} < 0.8$ V, corresponding to state 1/2, and a low level of $V_{out} \sim 0.15$ V for $V_{in} > 0.85$ V. The ternary device shown in this work is the first demonstration of how a multi-V_{th} design, enabled by ultrathin nature of 2D semiconductors and their heterojunction engineering, can be suited and ubiquitous for the design of efficient multivalued logic circuits.

In conclusion, to obtain a better understanding of band-to-band tunneling in MoS_2/WSe_2 hetero-FETs, the energy band diagram of the MoS_2/WSe_2 heterostructure was calculated and compared in the out-of-plane and in-plane directions to evaluate the possibility of band-to-band tunneling in different regions and directions. The results confirm that the effective heterojunction bandgap at the edge of the overlapped region of n-MoS_2 and p-WSe_2 in the horizontal direction is significantly smaller than their bandgap in the overlapped region in the out-of-plane direction. These results indicate that the band-to-band tunneling dominantly occurs at the edge rather than the, commonly believed, overlapped region of the MoS_2/WSe_2 heterojunction. Next, a tunnel-diode was designed and fabricated based on this heterostructure. We observe for the first time room-temperature NDR in a MoS_2/WSe_2 tunneling diode with an average conductance slope of 75 mV/dec and a large curvature coefficient of 62 V^{-1} at room temperature that highlights the remarkable potential of 2D crystals-based heterostructures for high performance tunneling transistors. Also, we have demonstrated MoS_2/WSe_2 van der Waals

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heterojunction transistors with negative differential transconductance. After gate dielectric optimization, as an application, the optimized transistor was then used to build a ternary logic inverter with three stable logic states operating with a supply voltage of V_{dd} = 1 V, which is the first demonstration of such electronic devices with 2D materials.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b04791.

Additional data concerning the MoS_2/WSe_2 heterostructure fabrication by dry transfer technique, optical characterization of the heterostructure, device fabrication, and band diagram calculations. (PDF)

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Notes

The authors declare no competing financial interest.

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Supplementary Information:

Transport Properties of a MoS_2/WSe_2 Heterojunction Transistor and its Potential for Application

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Heterostructure fabrication by dry transfer:

The heterojunction devices were prepared by the commonly used pickup and dry transfer methods[1,2]. WSe_2 and MoS_2 are mechanically exfoliated from commercially available bulk crystals using cleanroom grade on a separate pre-cleaned (i.e., Piranha solution, oxygen plasma and solvent cleaning) substrate. A polydimethylsiloxane (PDMS) sheet was cut into small pieces and placed on a pre-cleaned glass slide with double-sided tape. A 6% solution of polypropylene carbonate (PPC, Sigma Aldrich) in chloroform was then spin coated on the glass/tape/PDMS stack. This transfer slide was then loaded into the probe arm of the transfer setup and brought into contact with the desired flake at room temperature. The stage was then heated to 90 °C and maintained at that temperature for 1 min. After the temperature of the stage was returned to room temperature, by natural or forced cooling, the transfer slide was slowly disengaged. This process was repeated for the second flake. The picked-up heterostructure was transferred to the pre-

patterned via holes and heated up to 155 °C to release the polymer. Finally, the polymer was dissolved in chloroform followed by solvent cleaning and annealing (200 sccm Ar/200 sccm H_2) at 360 °C for 3 h.

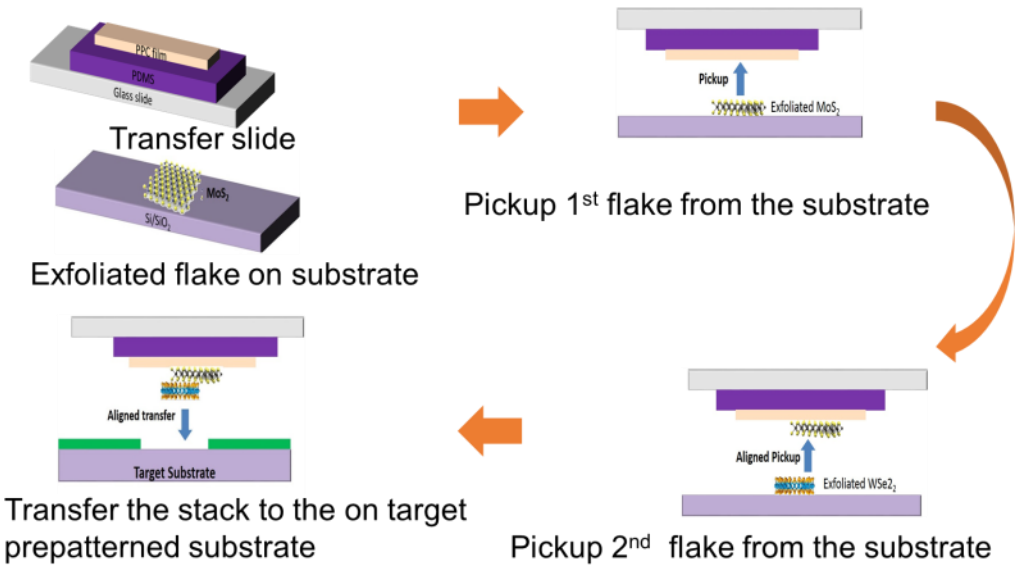

Figure S1: *Schematic of the heterostructure fabrication by the dry transfer method.*

Optical characterization of the MoS_2/WSe_2 heterostructure:

Supplementary Fig. S2 (a) and (b) respectively show the Raman and photoluminescence spectrum of the MoS_2/WSe_2 heterostructure in Supplementary Fig. S2 (c). The Raman spectra were obtained at the red, blue and purple marks in Supplementary Fig. S2 (c) for WSe_2 (4 layer), MoS_2 (2 layer) and the MoS_2/WSe_2 heterostructure, respectively, and are displayed with same colours as used in Supplementary Fig. S2 (a). The excitation laser wavelength was 532 nm with a beam spot size of approximately 1 μm. The Raman spectrum for MoS_2 (blue) shows the characteristic peaks of E_{2g} (~385 cm^{-1}) and A_{1g} (406 cm^{-1}) with a E_{2g}/A_{1g} peak intensity ratio of 1.56, and the Raman spectrum for WSe_2 (red) shows the major characteristic peaks of

E_{2g} (251 cm^{-1}) and A_{1g} (258 cm^{-1}) with a E_{2g}/A_{1g} peak ratio of 2.24 along with minor peaks at 309 cm^{-1}, 360 cm^{-1}, 375 cm^{-1} and 396 cm^{-1}. However, in the Raman spectrum of the heterostructure (purple), all the characteristics peaks of both MoS_2 and WSe_2 were observed but with reduced intensity. Supplementary Figure S2 (b) shows the photoluminescence characteristics of the sample at the same positions of Raman measurement. Because of the low number of MoS_2 and WSe_2 layers, and the indirect bandgaps of these semiconductors, the PL signal is relatively weak but we can observe a characteristic peak at 1.8 eV for MoS_2 and at 1.6 eV for WSe_2. In the overlap area, we observed the PL for both materials were quenched owing to exciton dissociation and charge transfer at the interface similar to the monolayer–monolayer junction results reported previously[3].

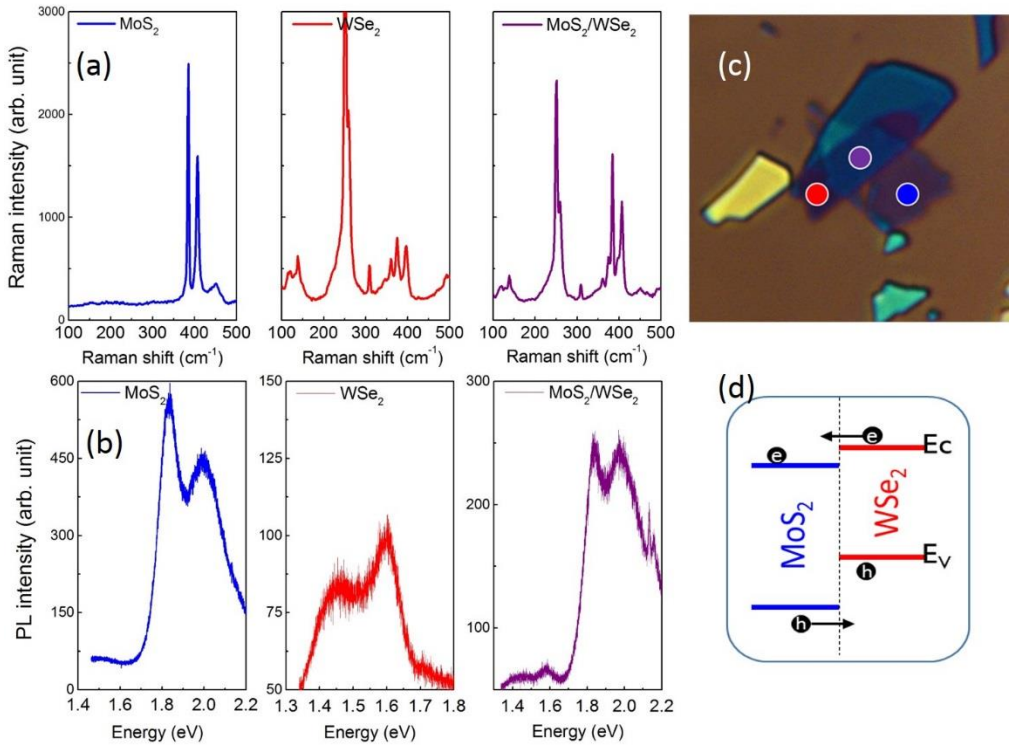

Figure S2: *(a) Raman spectrum of the sample taken at the different points marked in (c). (b) Photoluminescence spectrum of the sample at the same points marked in (c). (c) Optical image of the*

MoS_2/WSe_2 heterostructure used in this work. (d) Exciton dissociation mechanism at the heterojunction.

The photo response:

The light response of the device is reflected by the photoresponsivity ($\left(I_{light} - I_{dark}\right)/P_{incident}$) and photosensitivity ($\left(I_{light} - I_{dark}\right)/I_{dark}$), where I_{light}, I_{dark} and $P_{incident}$ are the current under illumination, dark current and incident power, respectively. Supplementary Figure S3 (a) shows the I_d vs V_g curves of the device in Figure 1 in the dark and under white light illumination with a power density of 0.03 W/cm^2 and the corresponding photoresponsivity (Supplementary Figure S3 (b)) and photosensitivity (Supplementary Figure S3 (c)). Under illumination, the current peak shifts from region **II** to region **I**. This shift can be attributed to the negative shift of the threshold voltage (V_{th}) in MoS_2-FETs arising from photo current generation in mono and few layer MoS_2. A similar trend was observed by Lopez-Sanchez *et al.*[4]. The device shows a high maximum photoresponsivity of 7 A/W and a photosensitivity of about 10^5 at V_g=-56 V (region **I**). The photoresponsivity then decreases monotonically in region **II**, while the photosensitivity decreases to unity and then increases to ~500 where it starts its exponential decrease in region **III** and finally decreases to sub-unity values, while the photoresponsivity increases exponentially and saturates about 450 A/W. Therefore, the conditions of region **I** of the MoS_2/WSe_2 device are best suited for photodetection applications.

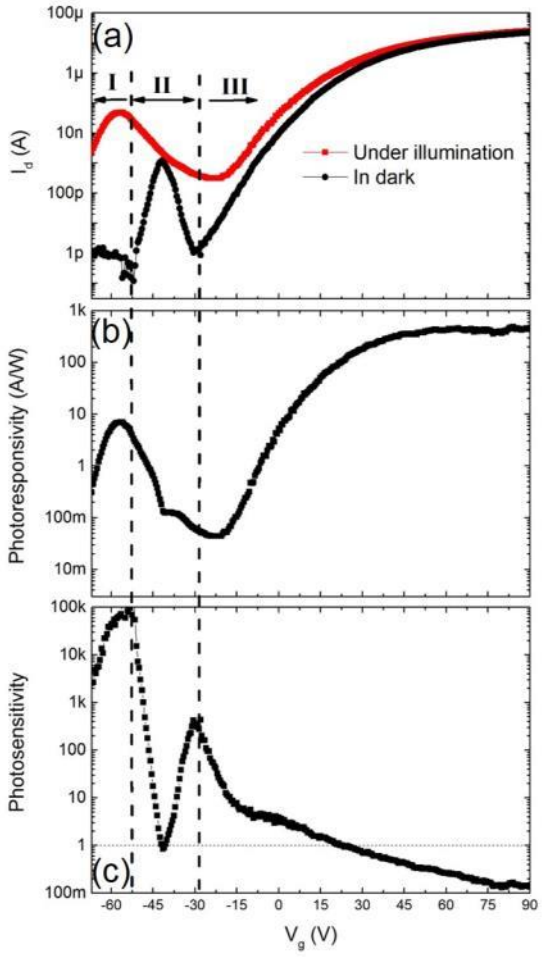

Figure S3: *(a) Transfer characteristics of the in-series MoS_2/WSe_2 hetero-FET (also shown in Figure 1(b)) in the dark and under illumination. (b) Photoresponsivity and (c) photosensitivity under a white light power intensity of 0.03 W/cm^2.*

Device fabrication:

Despite the interesting features observed in both operation modes of the hetero-FET of Figure 1, the gate efficiency (dE_F/dV_g) is very low, due to the very thick gate oxide (300 nm SiO_2) used in the device. Therefore, very large gate voltages are required to operate the transistors (-70 V$<V_g<$90 V). To date, 2D devices have mainly been limited to either single top-gated transistor or single back-gated transistor configurations with Si substrates acting as a global back gate, which are normally coated with a very thick SiO_2 layer as the dielectric. The reasons for using

such a thick oxide are twofold: to obtain sufficient optical contrast to locate micrometre-wide flakes, and to avoid large gate leakage, because the Si substrate is a global back gate with 100% overlap with the source/drain (S/D) contacts and the measurement pads.

To enhance the performance of the transistors and improve the gate efficiency, we need to increase the gate dielectric capacitance, whilst keeping the gate leakage current as low as possible. Herein, a simple solution is used to solve this problem: we fabricate the transistor channel on a thin high-k dielectric, for example, HfO_2, while the metal pads and wires are isolated using the thick SiO_2 layer. In this configuration, the transistor benefits from a global back gate that provides lower contact resistance, and the gate leakage current is also reasonably low.

For the scaled gate dielectric devices, 30 μm × 30 μm via holes are defined on a 90 nm SiO_2/Si substrate with electron-beam lithography. These via holes are then wet etched followed by an atomic layer deposition of 10 nm HfO_2 using tetrakis(dimethylamido)-hafnium (IV) and water at 250 °C. The sample is then annealed in forming gas at 400 °C to reduce the bulk oxide traps. The subsequent lithography steps are the same as in regular devices.

Supplementary Figure S4 shows a representative hetero-FET comprising MoS_2 and WSe_2 thin films contacted with Au and Pt lines. Measurement pads (not shown) and wide connecting lines are kept on a thick SiO_2 plateau and lines lying on the bottom of the SiO_2 via are kept below 400 nm in width to maintain a low gate leakage current.

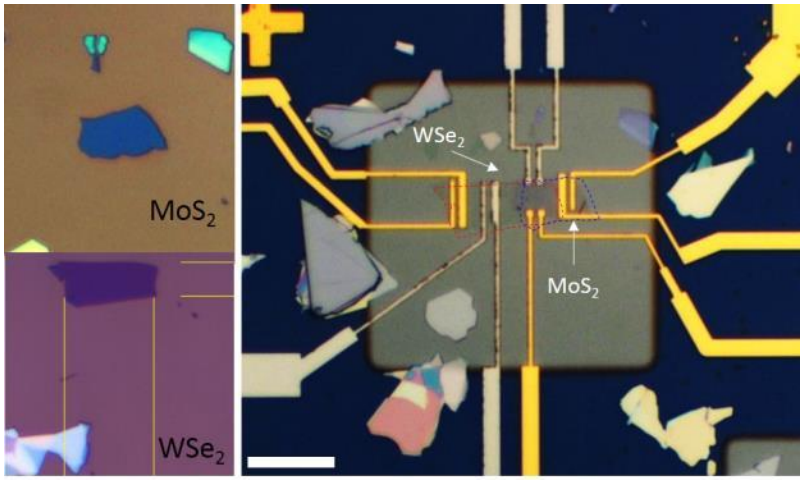

Figure S4: *Optical images of representative exfoliated MoS_2 and WSe_2 flakes as well as the final MoS_2/WSe_2 hetero-FET fabricated in a 90 nm deep SiO_2 via coated with 10 nm HfO_2. Flakes are contacted with Au and Pd. The scale bar is 10 μm.*

The transistor structure used in this work shows an average gate-leakage current $|I_{gate}|<100$ pA/μm in the measurement range, compared with $|I_{gate}|<1$ pA/μm for the device in Figure 1 with 300 nm SiO_2, effective oxide thickness (EOT)=300 nm. Supplementary Figure S5 shows the capacitance–voltage (C–V) characteristics of a generic multilayer MoS_2 capacitor with an Au electrode and Si substrate as the capacitor electrode and 10 nm HfO_2/native SiO_2 as the dielectric. The capacitor shows a clear transition from depletion to accumulation modes with EOT=3.3 nm. Heating the device to 360 °C in a H_2/Ar atmosphere resulted in sharper C–V curves owing to annealing of the MoS_2/HfO_2 interfacial defects.

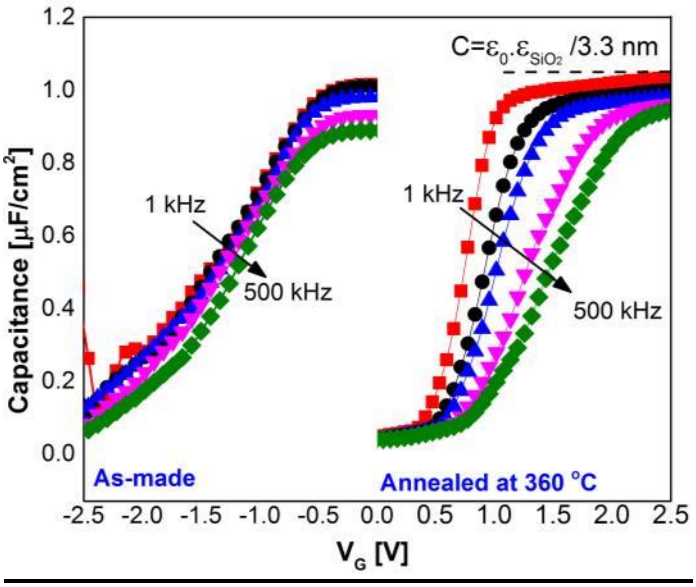

Figure S5: *As-made and after-annealing capacitance–voltage characteristics of a multilayer MoS_2 capacitor at different frequencies in the 1 to 500 kHz range.*

Supplementary Figure S6 (a) shows the schematic of a MoS_2-FET that was built in 90-nm-deep SiO_2. The transfer characteristics of a monolayer and a 4-layer MoS_2-FET are compared in Supplementary Figure S6 (b). The monolayer MoS_2 device shows a minimum sub-threshold swing (SS_{min}) of 71 mV/dec, while the multilayer device shows a SS_{min} of 105 mV/dec (Supplementary Figure S6 (c)). Here, $SS = (\frac{d(\log 10 I_d)}{dV_g})^{-1} \approx \ln\frac{kT}{q}(1+\frac{qD_{it}}{C_{ox}})$, where k is the Boltzmann constant, C_{ox} is the gate dielectric capacitance and D_{it} is the trap charge density at the dielectric/channel interface. For D_{it}=0, SS=60 mV/dec at room temperature, which is the thermionic limit of SS in conventional MOSFETs. The deviation of SS from 60 mV/dec in the monolayer MoS_2-FET can be attributed to the presence of trap charge density in the MoS_2/HfO_2 interface and the even larger SS in the multi-layer MoS_2-FET is further affected by the large inter-layer resistance and larger channel body in the multi-layer MoS_2 that lowers the electrostatic control of the gate over the channel. Supplementary Figure S6 (d) shows the I_d–V_g

plot of a parallel-mode MoS_2/WSe_2 hetero-FET. In contrast to the in-series mode (Figure 1 (c)), in the parallel mode, both source and drain electrodes are in contact with the overlapping MoS_2/WSe_2 region, forming a parallel bilayer FET's channel. In this configuration, the I_d–V_g curve resembles the sum of the I_d–V_g of two isolated MoS_2 and WSe_2 FETs. As depicted in Figure S6 (d), I_d–V_g has two almost symmetric electron and hole conduction branches with a narrow OFF-state region with I_{ON}/I_{OFF} in excess of 10^5 and SS_{min} of 110 mV/dec. In this configuration, at large positive V_g values, both MoS_2 and WSe_2 are in the electron accumulated mode and the channel is *n*-type. At large negative V_g values, the conduction is dominated by the *p*-type conduction of the WSe_2 component in the channel, while the MoS_2 sub-channel is depleted.

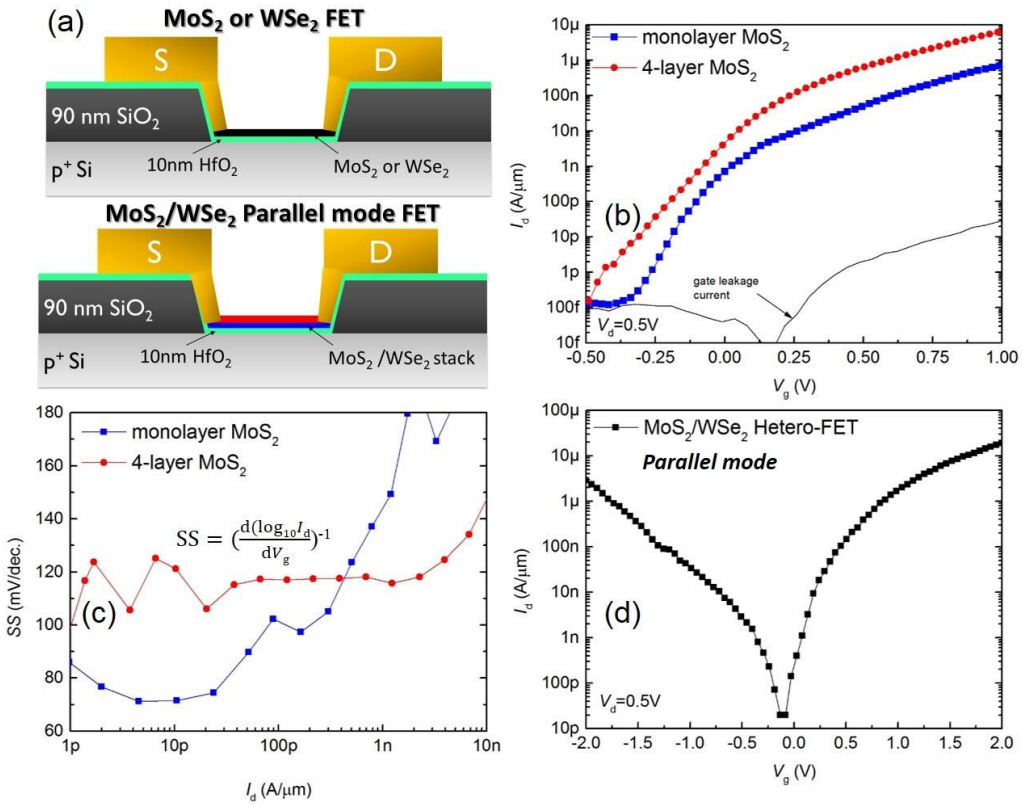

Figure S6: *(a) Schematic of a generic MoS_2 or WSe_2 FET and a MoS_2/WSe_2 hetero-FET in parallel mode using a thin HfO_2 gate dielectric with SiO_2 contact isolation. (b) I_d–V_g of the monolayer and 4-layer MoS_2-FETs. (c) Sub-threshold swing (SS) of the device shown in (b). (d) I_d–V_g of a representative MoS_2/WSe_2 hetero-FET. Here, the drain current I_d in (b) and (d) is plotted along the vertical axis and in (c) along the horizontal axis on a log scale.*

Band diagram calculations:

The band diagrams of the MoS_2/WSe_2 heterojunction in this work are obtained using the nextnano semiconductor nanodevice simulation tool[5]. An indirect bandgap of 1.2 eV is used for both MoS_2 and WSe_2 in the simulation, which is consistent with the reported experimental and theoretical bandgap values for few-layer and multilayer values[6]. In-plane masses of $m^*=0.46m_e$ and $m^*=0.33m_e$ are used for MoS_2 and WSe_2, respectively, and the out-of-plane mass of

$m^*=1.73m_e$ is used for multilayer films[8,9]. For dielectric constants, in-plane $\varepsilon_r=6$ and $\varepsilon_r=12$ and out-of-plane $\varepsilon_r=4$ and $\varepsilon_r=7$ are used for MoS_2[10,11] and WSe_2[12], respectively. In addition, according to the literature[6,7], a band offset of 0.4 eV between the conduction bands of multilayer MoS_2 and WSe_2 is included. The weak van der Waals interaction between the layers, owing to the random orientation of their lattices, leads to an effective vacuum potential barrier. Here, a vacuum barrier of 4 Å is considered in the MoS_2/WSe_2 heterostructure in Figure 2 as the van der Waals gap between the two films.

Figure 4 compares the in-plane and out-of-plane band diagrams of *n*-MoS_2/*p*-WSe_2 heterojunctions with three different combinations of thicknesses, all with the same electron and hole charge densities. The choice of electron and hole concentrations was based on typical values of naturally doped MoS_2 and WSe_2 extracted from their field effect transistors. The conclusion from Figure 4 was that for the given charge densities, a thickness-asymmetric heterostructure is required to achieve a small effective bandgap in the in-plane direction, which can enable band-to-band tunnelling. In Supplementary Figure S6, we compare the impact of different charge densities on the effective bandgap ($\Delta E_g=E_{c,MoS2}-E_{v,WSe2}$) for the best thickness choice in Figure 4, that is, 2 nm WSe_2/10 nm MoS_2. Three different combinations of charge densities were considered. As can be seen, to have a minimum ΔE_g, the hole concentration of WSe_2 (p) needs to be relatively larger than the electron concentration (n) of MoS_2 ($p>n$), while the opposite configuration ($p<n$) results in a relatively large ΔE_g and equal charge densities ($p=n$) shows a small ΔE_g but still larger than the $p>n$ case. As a conclusion of both Figure 4 and Supplementary Figure S7, the precise control of the thickness and charge density in the heterostructure components is essential to realize in-plane band-to-band tunnelling; however, regardless of the

choice of the thickness or the charge density of the two components, the effective bandgap in the out-of-plane direction remains relatively large (ΔE_g=0.8–0.9 eV) in MoS_2/WSe_2 heterojunctions.

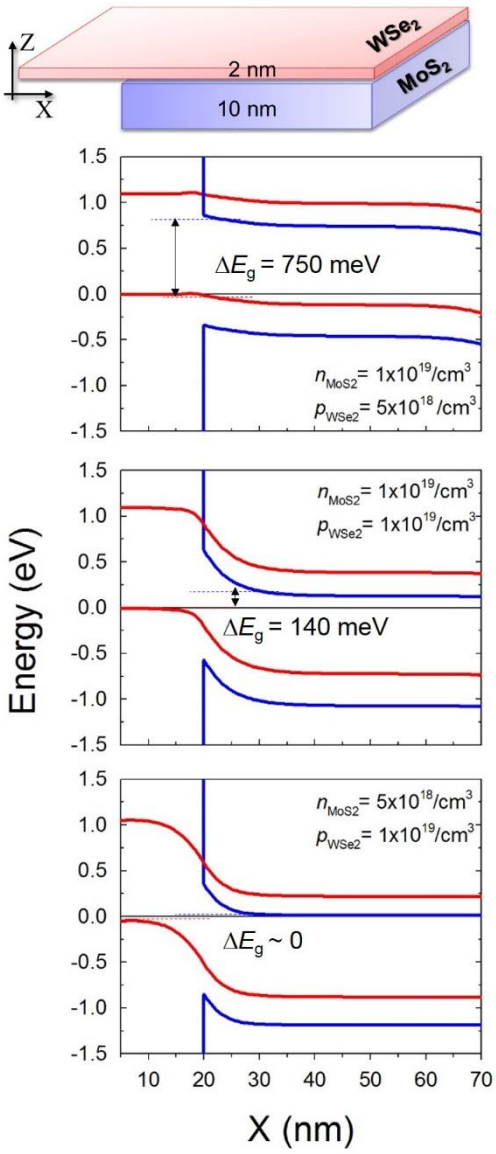

Figure S7: *Schematic of a 2 nm WSe_2/10 nm MoS_2 heterojunction and its calculated in-plane band diagrams with three different MoS_2 and WSe_2 charge concentration combinations.*

I_d–V_d characteristics of MoS_2/WSe_2 hetero-FETs:

Supplementary Figure S8 shows the plots of the I_d–V_d curves of MoS_2/WSe_2 hetero-FETs with different thicknesses, monolayer, few layer (2-4 layers) and multilayer (>4layers). As is discussed in the main manuscript, the thickness-asymmetric heterojunctions comprising few layer-WSe_2 and multilayer MoS_2 films are suitable for lateral-tunnelling devices. The representative devices in Supplementary Figure S6 show strong NDR. The variation is attributed to sample to sample variation in the natural doping of exfoliated flakes, as well as to imperfections induced by the transferring process. The monolayer MoS_2/few-layer WSe_2 shows diode behaviour with strong rectification, while few-layer/few-layer devices have larger reverse current.

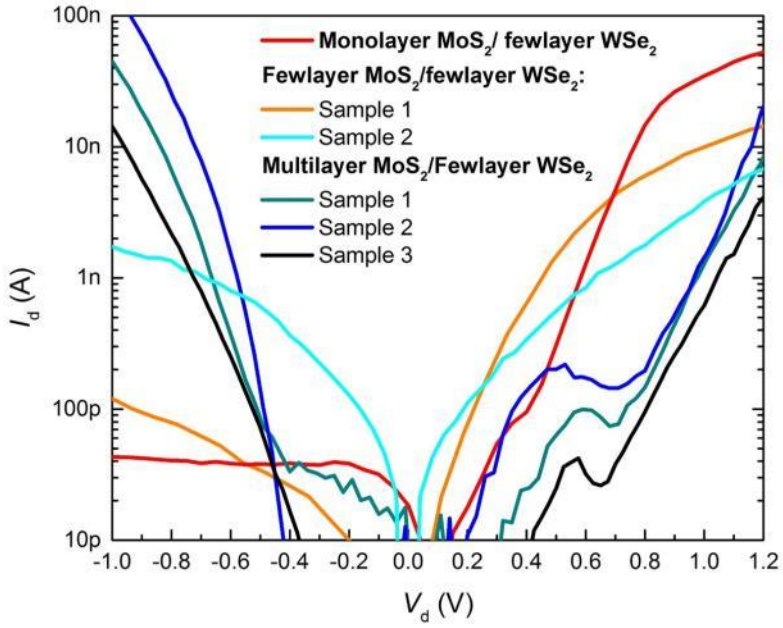

Figure S8: *I_d–V_d of several MoS_2/WSe_2 hetero-FETs with different MoS_2 and WSe_2 thicknesses fabricated in this work.*

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