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MoS_2 Field-Effect Transistor with Sub-10 nm Channel Length

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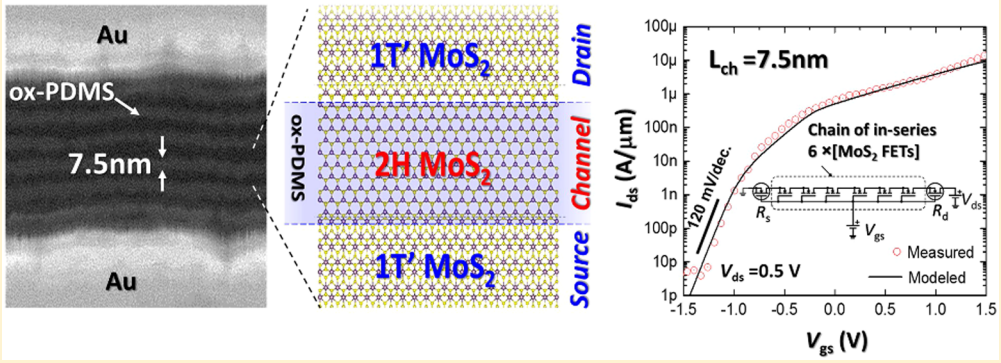
Supporting Information



ABSTRACT: Atomically thin molybdenum disulfide (MoS_2) is an ideal semiconductor material for field-effect transistors (FETs) with sub-10 nm channel lengths. The high effective mass and large bandgap of MoS_2 minimize direct source−drain tunneling, while its atomically thin body maximizes the gate modulation efficiency in ultrashort-channel transistors. However, no experimental study to date has approached the sub-10 nm scale due to the multiple challenges related to nanofabrication at this length scale and the high contact resistance traditionally observed in MoS_2 transistors. Here, using the semiconducting-to-metallic phase transition of MoS_2, we demonstrate sub-10 nm channel-length transistor fabrication by directed self-assembly patterning of mono- and trilayer MoS_2. This is done in a 7.5 nm half-pitch periodic chain of transistors where semiconducting (2H) MoS_2 channel regions are seamlessly connected to metallic-phase (1T′) MoS_2 access and contact regions. The resulting 7.5 nm channel-length MoS_2 FET has a low off-current of 10 pA/μm, an on/off current ratio of $>10^7$, and a subthreshold swing of 120 mV/dec. The experimental results presented in this work, combined with device transport modeling, reveal the remarkable potential of 2D MoS_2 for future sub-10 nm technology nodes.

KEYWORDS: *MoS_2 FETs, sub-10 nm, phase transition, block copolymers, virtual source modeling*

As the channel length of transistors has shrunk over the years, short-channel effects have become a major limiting factor to transistor miniaturization. Current state-of-the-art silicon-based transistors at the 14 nm technology node have channel lengths around 20 nm, and several technological reasons are compromising further reductions in channel length. In addition to the inherent difficulties of high-resolution lithography, the direct source−drain tunneling is expected to become a very significant fraction of the off-state current in sub-10 nm silicon transistors, dominating in this way the standby power. Therefore, new transistor structures that reduce the direct source−drain tunneling are needed to achieve further reductions in the transistor channel length. Transistors based on high mobility III−V materials,[1,2] nanowire field-effect transistors (FETs),[3,4] internal gain FETs[5,6] (such as negative capacitance devices), and tunnel FETs[7] are among those that have been considered to date. More recently, layered 2D semiconducting crystals of transition metal dichalcogenides (TMDs), such as molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2), have also been proposed to enable aggressive miniaturization of FETs.[8−11] In addition to the reduced direct source−drain tunneling current possible in these wide-bandgap materials, the atomically thin body of these novel semiconductor materials is expected to improve the transport properties in the channel thanks to the lack of dangling bonds. Some studies have reported, for example, that single-layer MoS_2 has a higher mobility than ultrathin body silicon[12] at similar thicknesses.

Moreover, the atomically thin body thickness of TMDs also improves the gate modulation efficiency. This can be seen in

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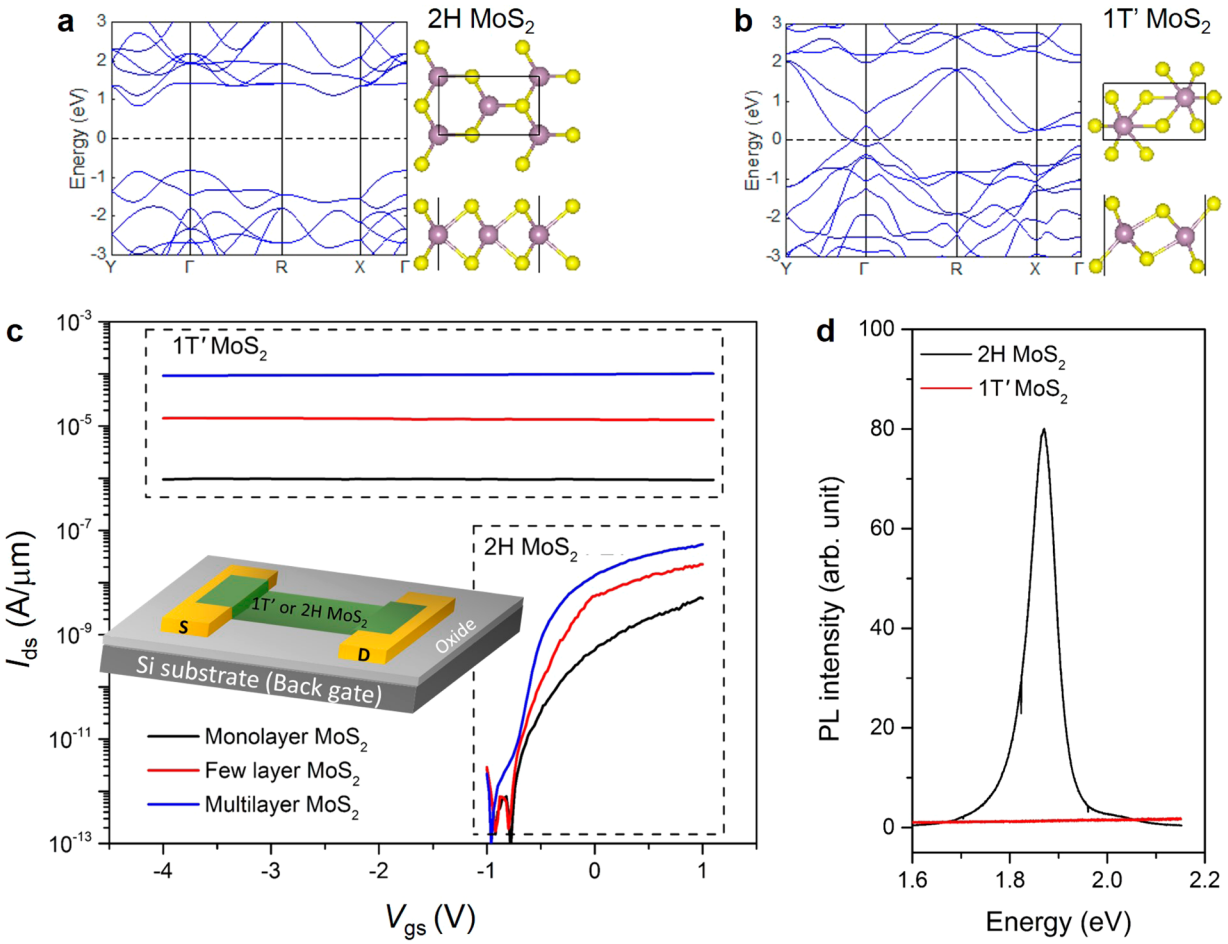

Figure 1. (a, b) Electronic band structures of 2H and 1T′ MoS_2 and their atomic structures. The 2H band structure shows a bandgap of approximately 1.8 eV, while the conduction and valence bands of 1T′ MoS_2 are overlapped; therefore, 1T′ MoS_2 has metallic gapless characteristics. (c) Transfer characteristics of three MoS_2 FETs with different thicknesses of MoS_2 before and after phase transition treatment. The intrinsic 2H MoS_2 FETs show strong semiconducting behavior with large gate modulation, while all of them after the phase transition show constant current, increasing with thickness, with almost no gate modulation featuring metallic 1T′ MoS_2. (d) PL spectra of monolayer 2H and 1T′ MoS_2. The 2H phase shows a strong PL peak at 1.85 eV generated by its bandgap, while the PL of the 1T′ phase is completely quenched owing to its gapless metallic characteristics. See Supporting Information S1 and S2 for CVD growth of monolayer MoS_2 and Raman characteristics of different phases of MoS_2, respectively.

their characteristic scaling length,[13] $\lambda = \sqrt{\frac{\varepsilon_{semi}}{\varepsilon_{ox}} t_{ox} t_{semi}}$, which determines important short channel effects such as the drain-induced barrier lowering (DIBL) and subthreshold swing (SS). In particular, MoS_2 has low dielectric constant $\varepsilon = 4-7$[14,15] and an atomically thin body ($t_{semi} \approx 0.7$ nm × number of layers), which facilitate the decrease of λ, while its relatively high bandgap energy (1.85 eV for a monolayer) and high effective mass allow for a high on/off current ratio (I_{on}/I_{off}) via reduction of direct source−drain tunneling.[16] These features make MoS_2 in particular, and wide-bandgap 2D semiconductors in general, highly desirable for low-power subthreshold electronics. In these applications, the on-current (I_{on}) for a given I_{off} is influenced more by the subthreshold swing (SS) than by the carrier mobility.

To demonstrate and benchmark MoS_2 transistors with channel lengths below 10 nm, two important challenges need to be overcome. First, a suitable lithography technology is required. Then a low-contact resistance is needed for the source and drain access regions to ensure that the channel resistance will dominate the device behavior. In this work, to reduce the contact resistance, we used a junction between the metallic phase of MoS_2 (1T) and its semiconducting phase (2H).[17−19] The atomic and electronic-band structures for the two phases are shown in Figure 1, panels a and b, as obtained from density functional theory (DFT). The transition from the 2H- to the 1T-phase can be triggered by exposing 2H MoS_2 to *n*-butyllithium (*n*BuLi) solution.[20] The pure 1T-phase is unstable and undergoes a structural transition to the dynamically stable 1T′-phase.[20] Figure 1, panel c compares the transfer characteristics (i.e., drain−source current vs gate−source voltage, $I_{ds}-V_{gs}$) of a MoS_2 FET before (2H-phase) and after (1T′-phase) phase-transition treatment of its channel layer. The metallic character of the 1T′ MoS_2 channel prevents any current modulation by the gate electrode. This is in contrast to the large modulation observed for the semiconducting 2H-MoS_2 channel. Photoluminescence (PL) spectra of monolayer 2H- and 1T′ MoS_2 are shown in Figure 1, panel d. The 2H-phase displays a strong PL peak at 1.85 eV originating from its bandgap, while the PL of the 1T′-phase is fully quenched because of its gapless metallicity.

The two MoS_2 phases can, in fact, coexist by forming a stable boundary between the phases.[18,20,21] Selective conversion of 2H MoS_2 to 1T′ MoS_2 by locally masking with poly(methyl

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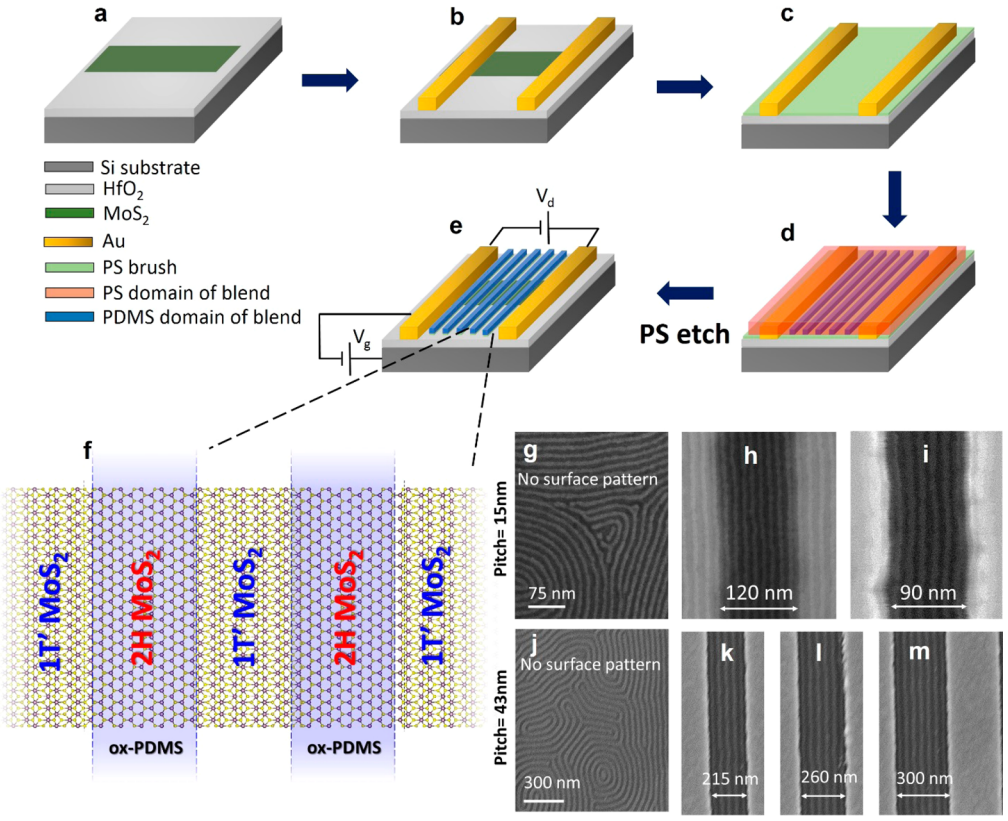

Figure 2. (a) Deposition of MoS_2 on a HfO_2-coated Si wafer (see Supporting Information S3, for details of substrate preparation) is followed by (b) Au metallization by e-beam lithography to form contacts to MoS_2. These contacts are used as the S/D electrode in the long channel MoS_2 FET (before phase transition treatment) and as the end-contacts for the chain of 2H/1T′ MoS_2 FETs (after the phase transition). Next, (c) MoS_2 is functionalized with a PS brush and then (d) spun PS-*b*-PDMS BCP followed by an annealing step that leads to microphase separation of the blocks and finally (e) selective etching of the PS and leave ox-PDMS patterns on the substrate. After that (not shown here; see Supporting Information S4 for details), the sample will be treated with nBuLi for 2H to 1T′ phase transition in the nonprotected regions. (e) Biasing schematic of the MoS_2 chain FETs, where the Si substrate is used as the back-gate and the Au electrodes are used as end contacts; (f) schematic of the patterning in the 1T′ and 2H MoS_2 sequencing regions. SEM images show PDMS lines with (g–i) 15 nm and (j–m) 43 nm pitches after PS etching on surfaces with no guide pattern as well as surfaces with Au lines with different spacings to act as guides. The absence of a guide pattern leads to random formations of the PDMS lines, while in patterned surface lines are self-assembled (in parallel) with the Au electrodes.

methacrylate) (PMMA) and exposure to *n*-butyllithium (*n*BuLi) solution was used by Kappera et al.[20] to demonstrate 1T′ MoS_2/2H MoS_2/metal ohmic contacts with much smaller resistance than that of the 2H MoS_2/metal contacts. A variation of this technology was used in our work to form sub-10 nm 2H MoS_2 regions that act as FET channels sandwiched between adjacent 1T′ MoS_2 layers that reduce the access resistance to the FET channels. This seamless 2H/1T′ MoS_2 junction has a sharp atomic interface, which reduces both the physical separation between the two materials and the tunnel barrier and thus reduces the contact resistance.[22,23]

Lithography is the second challenge when realizing ultrashort channel MoS_2 transistors. Electron beam lithography can potentially provide sub-10 nm patterning resolution; however, it has low throughput, and it is not easy to control at these dimensions. An alternative technology is directed self-assembly (DSA) of block copolymer (BCP), which has a great potential for cost-effective, nanoscale, and high-volume manufacturing. The directionality of the features in the BCP films can be defined by physical or chemical templates created by conventional lithography.[24] A few functional devices have been fabricated to-date using BCP including 29 nm pitch silicon FinFETs.[25] Herein, the BCP-based technique is used for the first time to pattern an MoS_2 layer in its metallic and semiconducting phases with sub-10 nm resolution.

To form the self-assembled BCP lines, two different poly(styrene-*b*-dimethylsiloxane) (PS-*b*-PDMS) BCPs were used in this work, 45.5 kg/mol (SD45; fraction of PDMS, f_{PDMS} = 32%, period L_0 = 43 nm) and 10.7 kg/mol (SD10; f_{PDMS} = 25%, L_0 = 15 nm). The choice of this BCP was dictated by its high Flory–Huggins interaction parameter, as compared to other typical BCPs, such as poly(styrene–PMMA) (PS–PMMA). The high Flory–Huggins interaction parameter enables lower line edge roughness and a smaller period. In addition, there is a high etch selectivity between the two blocks, PS and PDMS. By using an oxygen plasma, the organic part (PS) can be easily removed, while the inorganic part (PDMS) shows high resistance to etching. The key processing steps are summarized in Figure 2, panels a–e. The critical step is the etching of PS regions (step 'e'). One must ensure that the plasma etching of PS is terminated before the MoS_2 thin films are destroyed. For this purpose, we developed an optimized etching procedure involving an initial direct oxygen plasma exposure to etch away the main portion of the PS blocks, followed by indirect plasma exposure to carefully etch the remaining PS. Details of the optimized plasma etching process are presented in Supporting Information S4.

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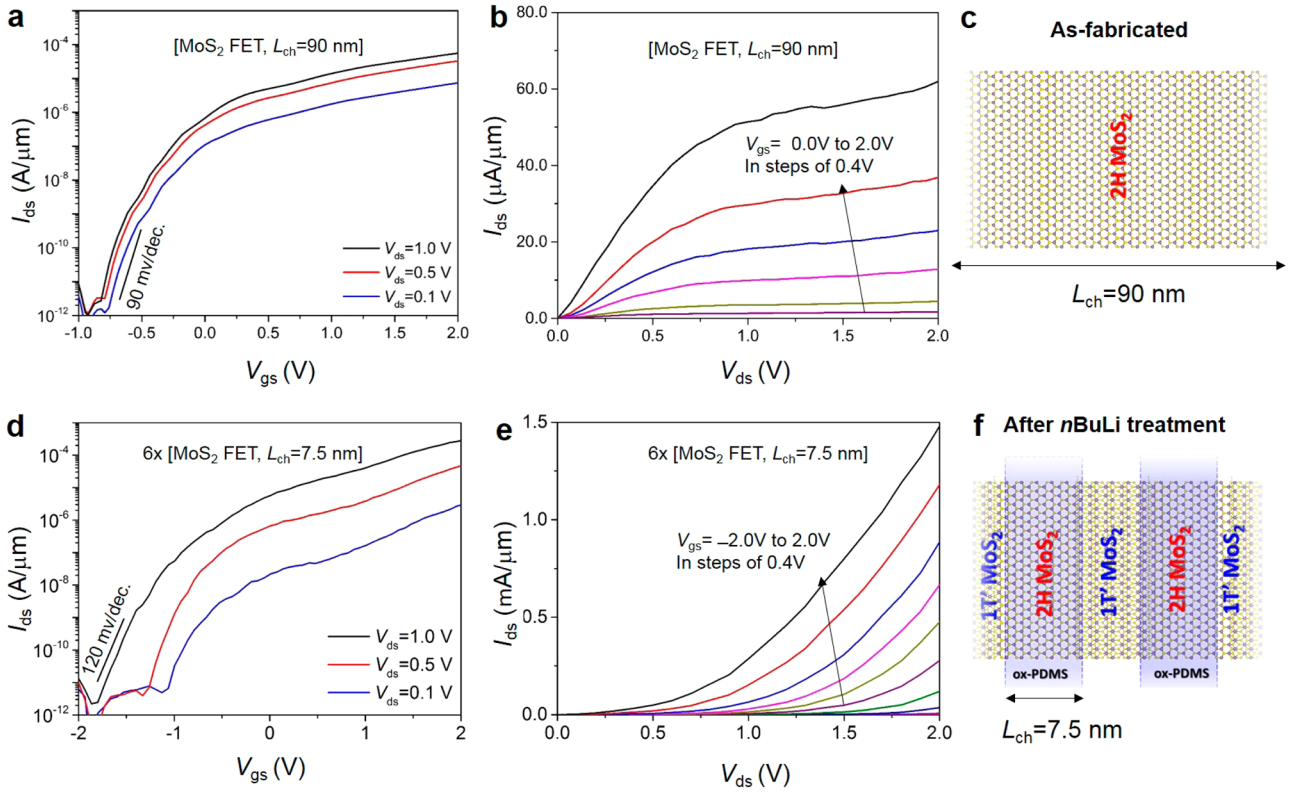

Figure 3. (a, b) $I_{ds}-V_{gs}$ and $I_{ds}-V_{ds}$ of an as-fabricated trilayer MoS_2 FET with channel length of 90 nm and EOT of 4 nm. (c) Schematic of 2H MoS_2 channel. (d, e) The same set of $I-V$ curves for the chain of six 7.5 nm MoS_2 in-series FETs produced after a phase transition treatment with *n*BuLi. The device demonstrates an I_{on}/I_{off} of $\sim 10^7$, low I_{off} of ~10 pA/μm, and a subthreshold slope of 120 mV/dec for more than two decades. The transfer characteristics in panel d exhibit a DIBL of 0.7 V/V, which results in the lack of saturation in the drain current in panel e. As discussed in the modeling section, this DIBL can be significantly suppressed by solely decreasing the EOT and thus enhancing the electrostatic control with the gate. (f) Schematic of alternating 2H/1T′ MoS_2 regions.

Figure 2, panels g–m show SEM images of self-assembled BCP lines with pitches of 43 and 15 nm formed between Au lines that serve as end-contacts to the MoS_2 film to form the external source/drain (S/D) electrodes. The patterned MoS_2 channel was then exposed to *n*BuLi and rinsed thoroughly to selectively convert the uncovered underlying 2H MoS_2 to 1T′ MoS_2, while the BCP-covered regions remained semiconducting thus forming a chain of transistors in series where each transistor is composed of a semiconducting channel and two adjacent metallic regions forming its immediate S/D contacts (see schematic in Figure 2f). The length of each one of these three regions is anticipated to be equal to the half-pitch of the BCP lines, which is either 7.5 or 22 nm, depending on the original pitch (15 nm vs 43 nm). The minimum number of 7.5 nm lines formed between a pair of 90 nm-spaced Au electrodes was six, while a minimum of five 22 nm lines were formed between Au lines spaced by 215 nm.

In this work, exfoliated MoS_2 flakes as well as chemical vapor deposition (CVD)-grown monolayer MoS_2 were used. The CVD technique used here is compatible with advanced device fabrication technologies and can provide full substrate coverage under optimized conditions; however, CVD-grown MoS_2 currently suffers from high density of structural defects. Conversely, exfoliated MoS_2 flakes have a much lower defect density but are very small in size; only tens of micrometers in diameter. MoS_2 flakes also allow the fabrication of transistors with few-layer-thick MoS_2 channels, which can potentially stand the damage induced by plasma treatment better than monolayer CVD MoS_2 because only the topmost layer is affected by plasma treatment. Here we focus on the experimental performance of a device with 7.5 nm channel length constructed on exfoliated trilayer MoS_2, which exhibits the best performance and shortest channel length among the fabricated devices. Details of CVD monolayer devices with 7.5- and 22 nm channel lengths are provided in the Supporting Information S5. In all studied devices, highly doped Si substrates with a 10 nm of HfO_2 layer on the surface are used as the back-gate stacks. The device fabrication process is described in detail in Supporting Information S3. Figure 3 shows $I_{ds}-V_{gsgs}$ and $I_{ds}-V_{ds}$ characteristics of a trilayer MoS_2 FET at different processing steps. As shown in Figure 3, panels a and b, the as-fabricated device with channel length of 90 nm shows good subthreshold characteristics with small DIBL< 0.1 V/V, SS = 88 mV/dec, and current saturation in $I_{ds}-V_{dsds}$ characteristics owing to velocity saturation.

The chain of in-series 7.5 nm MoS_2 FETs, formed after the *n*BuLi treatment, shows a well-defined $I_{ds}-V_{gsgs}$ performance with an I_{on}/I_{off} ratio in excess of 10^7 with SS_{min} of 120 mV/dec and I_{on} of 0.25 mA/μA at V_{ds} = 1 V (Figure 3d). These characteristics are further explored using device modeling in the discussion that follows. Thanks to the extremely thin body thickness and the wide bandgap of the MoS_2 channel, the short channel length of this device has a minimum impact on its subthreshold characteristics and the off-state current, I_{off} < 10 pA/μm. However, compared with the $I_{ds}-V_{gs}$ characteristics of the long channel (Figure 3a), the device shows larger DIBL of ~0.7 V/V. This also leads to the absence of saturation in the

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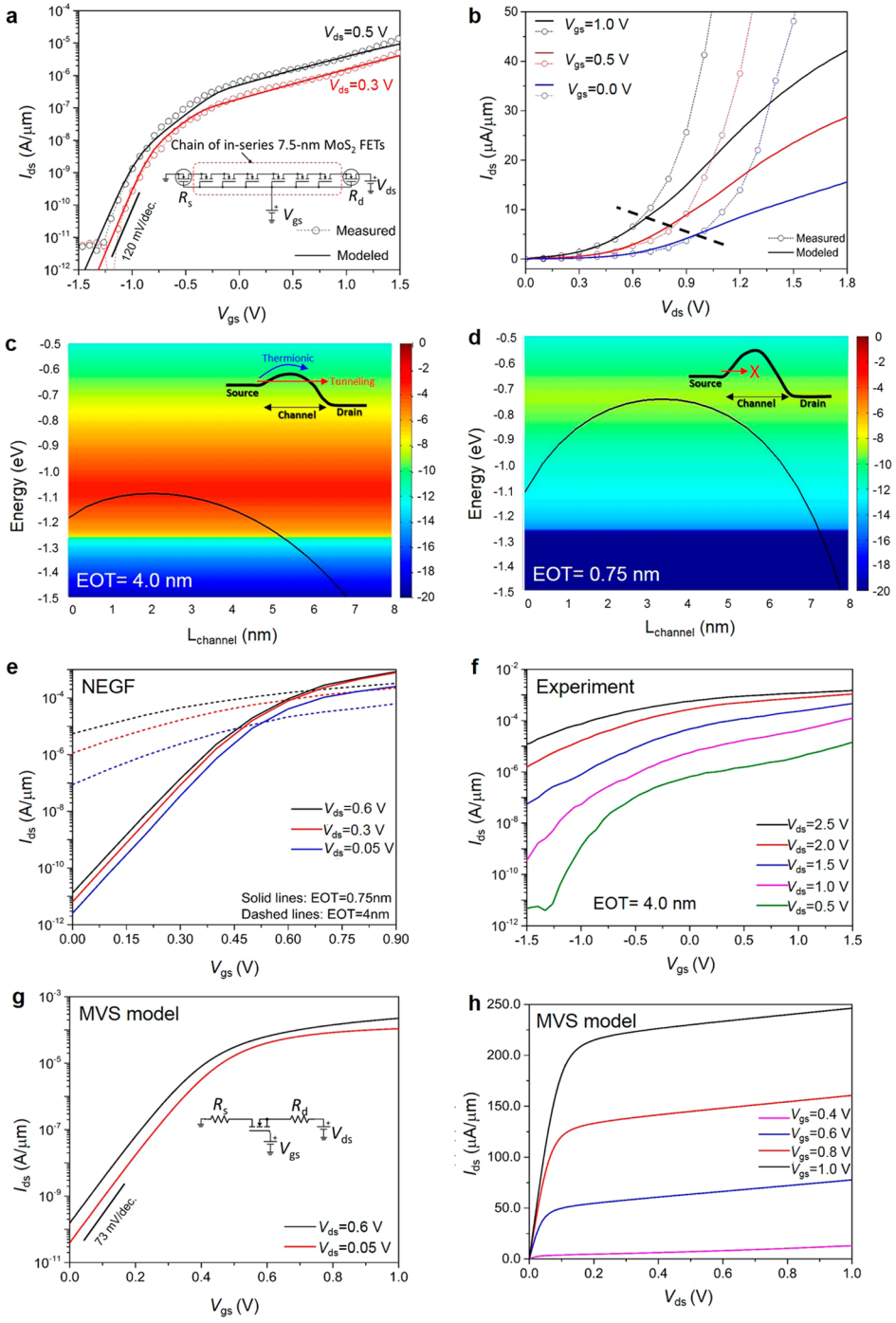

Figure 4. (a, b) MVS fit of the transfer and output characteristics. I_{ds}−V_{ds} fits the model well for V_{ds} < 0.6 V. At higher voltages, the direct source-to-drain tunneling becomes substantial. The dashed line in panel b is intended as a visual guide to indicate the two regimes. The inset in panel a shows the circuit configuration used in the MVS model consisting of a chain of six 7.5 nm MoS_2 FETs and V_{gs}-dependent R_s and R_d. (c) Energy-resolved total transmission probability T (scale is in $\log_{10}(T)$ and T is in units of nm^{-1}) from NEGF simulation for EOT of 4 nm, showing substantial tunneling through the barrier in the off state with high drain bias of V_{ds} = 0.6 V. (d) T for EOT of 0.75 nm, where the tunneling current this time is suppressed by orders of magnitude. Insets in panels c and d schematically illustrate the tunneling and thermal emission currents (e) transfer characteristics from NEGF for two different EOTs, showing significantly improved subthreshold slope and DIBL for the EOT of 0.75 nm. (f) Experimental I_{ds}−V_{gsgs} curves of the chain of 7.5 nm MoS_2 FETs at different values of V_{ds} showing substantial increase of I_{off} with increasing V_{ds}, in agreement with the modeling in panel e. (g, h) MVS prediction of transfer and output characteristics, taking into account the mobility, injection velocity, and resistance found in panels a and b. EOT of 0.75 nm is used. DIBL (72 mV/V) and subthreshold slope (~73 mV/dec.) are taken from panel e. See Supporting Information S6 for details of the MVS and NEGF models.

I_{ds}−V_{ds} curves (Figure 3e) despite the high current density in the mA/μm range, which is rather high for MoS_2 transistors.

To further analyze the performance of the sub-10 nm MoS_2 channels, we used the MIT Virtual Source Compact model (MVS)[26] to fit the experimental data for the MoS_2 FETs. In the past, the MVS model has been applied to short channel silicon,[26] III−V semiconductors,[27−29] and graphene[30] to extract device parameters such as injection velocity, carrier mobility,

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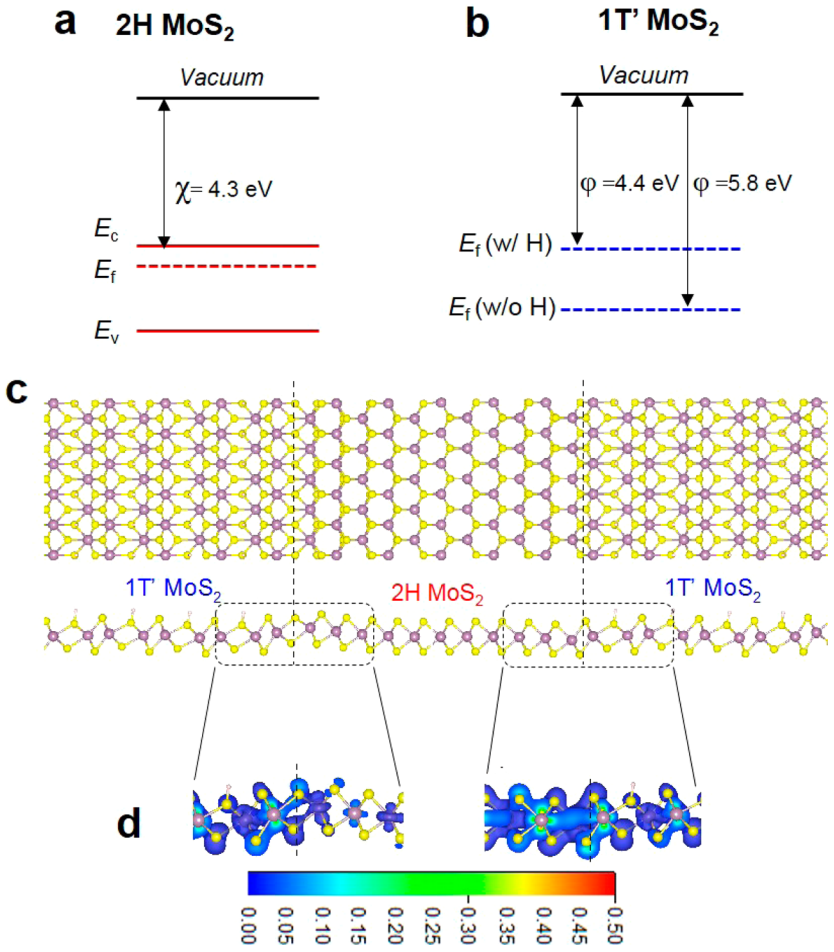

Figure 5. (a) Band diagram of 2H MoS_2. The calculated electron affinity value is χ = 4.3 eV. (b) Calculated work function (φ) values of 1T′ MoS_2 with and without the H functional groups. (c) Calculated atomic structure of 2H/1T′ MoS_2 boundary with H adsorbed on the 1T′-phase. To reduce the computational cost, we modeled alternating ∼3 nm-long 1T′-phase and ∼3 nm-long 2H-phase layers. (d) Contour plots of partial charge densities associated with the states in the energy range of [E_F−1.0 eV, E_F] at the two boundaries between the 1T′- and 2H-phases. The numbers in the color bar are in units of e/Å^3. The isosurface levels are selected at 0.02 e/Å^3. The partial charge density distribution on the side of the 1T′ phase is very similar at the two boundaries (see Figure S14 for the entire device), while on the 2H-phase side, the different edge (Mo-edge and S-edge) termination results in distinctly different density distributions. See Supporting Information S7 for details of DFT calculations.

and access resistance (which is equivalent to the 2H/1T′ junction resistance in this work). Here, gate capacitance, channel length, DIBL, and subthreshold swing are directly determined from the experimental data, while the remaining parameters (carrier mobility and velocity) are extracted by best-fitting the full I−V data. In addition to the chain of MVS-model-standard 2H/1T′ FETs in series, we also model the nonlinear gate voltage-dependent Au-MoS_2 contact resistance (R_s and R_d) at the external source and drain regions as two additional transistors in series with the chain of transistors. Figure 4, panels a and b compare the experimental transfer and output characteristics of the trilayer MoS_2 chain of in-series FETs with the model fitting. The parameters of the contact-modeling transistors were used purely as fitting parameters here; however, we found that the resulting contact resistance and its gate voltage dependence are well matched with the experimental Au-MoS_2 contact resistance data extracted in this work (Supporting Information S6). The injection velocity (v_{xo}) and the mobility are found to be ∼1 × 10^6 cm/s and 25 cm^2/V s, respectively. This mobility is the Matthiessen combination of diffusive and ballistic mobility, which gives the mean free path to be around 2.1 nm. The access resistance (where r_s = r_d = $r_{2H/1T'}$) is as low as 75 Ω μm, which indicates the ohmic nature of the 2H/1T′ junction; this aspect will be further discussed later in this work. The device also has a very low I_{off} (<10 pA/μm) and high I_{on}/I_{off} ratio, in good agreement with previous theoretical expectations.[31,32] This is a result of the ability of MoS_2 to suppress direct source−drain tunneling thanks to its high effective mass.

The lack of saturation in the I_{ds}−V_{dsds} characteristics and the deviation of the current from the MVS model (for V_{ds} > 0.6 V) as indicated in Figure 4, panel b, are mainly because of large DIBL induced by the relatively large effective oxide thickness (EOT) used in this work (∼4 nm, vs ∼0.8 nm in state-of-the-art CMOS technology). To clarify this point, we performed quantum mechanical simulations using nonequilibrium Green's function (NEGF) formalism for a single 7.5 nm MoS_2 FET. For the thicker oxide (4 nm EOT, Figure 4c), the barrier at the off-state (V_{gs} = 0) with high drain bias (V_{ds} = 0.6 V) is low enough to cause both high thermal emission currents and direct source−drain tunneling. This is in good agreement with the experiments (Figure 4f); however, it should be noted that as the experimental device has six transistors in series, it takes roughly six times the voltage drop across one transistor to

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produce the same level of tunneling current predicted by the simulation. It should be noted that for low V_{ds} values (up to ~0.6 V), the tunneling contribution is negligible (less than 10%) and the transport is determined by thermal emission.

NEGF simulations of a thinner oxide (0.75 nm EOT) predict a significant reduction in the transmission probability of at least five orders of magnitude both below and above the barrier (Figure 4d). This is because the barrier height is now higher and the potential reaches the peak much more quickly thanks to the lower scaling length. The effective mass of MoS_2 is large enough to reduce DIBL for the 0.75 nm EOT to approximately 72 mV/V and the subthreshold slope to about 73 mV/dec, as shown in Figure 4, panel e.

Figure 4, panels g and h show the MVS-calculated transfer and output characteristics of a single 7.5 nm MoS_2 transistor, as modeled using the DIBL and subthreshold slope parameters extracted from the NEGF simulation with a 0.75 nm EOT and V_t = 0.5 V (Figure 4e). In these simulations, the velocity, mobility, and resistance ($r_{2H/1T'}$ = 75 Ω μm) were taken from the MVS fit of the trilayer device. The device shows an I_{on}/I_{off} in excess of 10^6 with I_{off} as low as ~100 pA/μm and I_{on} of ~230 μA/μm at V_{gs} = 0.6 V. These numbers are not far from the requirements envisaged in the International Technology Roadmap for Semiconductors (ITRS)[33] for the 2024 low-power devices node (L_g = 7.5 nm, I_{on} = 400 μA/μm, I_{off} = 10 pA/μm). Further improvements in both the contact resistance and the on current are required, however, which may be made possible by the development of better MoS_2 growth techniques.

Finally, we would like to highlight two important points about the 2H/1T′ junction that must be addressed. The first is the stability of the 1T′ phase and the stability of its junction with the 2H phase, and the second is the formation of an ohmic interface, that is, a low barrier contact between the two phases that allows the 1T′ regions to act as suitable source or drain contacts to the 2H MoS_2 channel. Because MoS_2 FETs are *n*-type, these contacts must have a low work function to form effective ohmic contacts. To determine whether or not the 2H/1T′ MoS_2 junctions fulfill these requirements, we performed DFT calculations of the 2H MoS_2 phase and of both pristine and functionalized 1T′ phases and their junctions. The pristine 1T′ phase has a high work function of 5.8 eV when compared with the electron affinity of 2H MoS_2, which is ~4.3 eV as shown in Figure 5, panels a and b. Such a large energy difference would form a significantly high Schottky barrier for both MoS_2 thicknesses and would impede the formation of an ohmic contact. However, as shown by the experimental results, $r_{2H/1T'}$ is relatively small (~75 Ω μm), thus demonstrating the ohmic nature of the 2H/1T′ junction. To understand this apparent contradiction, we must assess the effects of surface adsorbates or functional groups in changing the charge density and thus the work function of 1T′ MoS_2. In fact, the adsorption of chemical species on the surface of 2D materials is known to modify their electronic properties. Given the chemical phase transition treatment that is applied in this work, which involves the formation of a lithium molybdenum sulfide (Li_xMoS_2) intermediate compound that requires a hydration reaction to remove the lithium content, the most probable adsorbates are hydrogen (H) functional groups.[17] Therefore, we used DFT calculations to study the properties of H-doped 1T′ MoS_2, where the H atoms are bonded to the sulfur atoms, which is the most favorable configuration. The results showed that H adsorption leads to further structural stabilization of the 1T′ phase. The pristine 1T′ phase is less stable than the 2H phase by 0.55 eV per MoS_2 molecule, but it becomes more stable by 0.16 eV per MoS_2 molecule with full H coverage of 0.5/Mo. We then constructed an atomic model and performed a structural relaxation analysis of the 2H/1T′ MoS_2 junction with H adsorbed on the 1T′ region only. The results showed that each phase remained stable after optimization and formed a stable boundary, which is in good agreement with the results of previous direct observations of 1T′ and 2H phases in coexistence.[20] The relaxed atomic structure of their boundary are shown in Figure 5, panel c. We note that a recent theoretical work[34] reported the structural stability and electronic properties of a similar structure between the S-edge 2H MoS2 and 1T′ MoS_2. Here, we observed that H adsorption raises the Fermi level and therefore substantially reduces the work function of 1T′ MoS_2 to about 4.4 eV at 0.5 H/Mo coverage, which eases ohmic contact formation by significantly reducing the energy barriers; this may also explain the small resistance observed in the 2H/1T′ junction. More details about the effects of H adsorption as well as other functional groups, for example, oxygen and hydroxyl (−OH) groups, on the stability and electronic structure of the 1T′ phase are presented in the Supporting Information S7. We also calculated the partial charge densities at the boundaries between 2H MoS_2 and H-functionalized 1T′ MoS_2 as shown in Figure 5, panel e. The calculations show that the electronic states closest to the Fermi level are not only from the metallic 1T′ phase, but also contain a substantial contribution from the atoms closest to the boundary in the semiconducting 2H phase. This lateral orbital overlapping, which stemmed from the seamless 2H/1T′ interface, further guarantees the ease of electron transition across the 2H/1T′ side-contact.

In summary, we have demonstrated the smallest MoS_2 transistor fabricated to date by aggressive channel length scaling to the sub-10 nm regime using DSA patterning of mono- and trilayer MoS_2 in a periodic chain of junction semiconducting (2H) and metallic-phase (1T′) MoS_2 regions with a half-pitch of 7.5 nm. The MoS_2 composite FET had an I_{off} of 10 pA/μm and an I_{on}/I_{off} in excess of 10^7. Modeling of the device current−voltage characteristics revealed that the 2H/1T′ MoS_2 junction has record-low resistance of 75 Ω μm, while trilayer 2H-MoS_2 exhibits a low-field mobility of ~25 cm^2/V s and a carrier injection velocity of ~10^6 cm/s. DFT calculations of the 2H/1T′ junction further confirmed the stability of the interface and indicated its ohmic nature. These results highlight the great promise of MoS_2 transistors fabricated at the limit of the ITRS technology roadmap.

Methods. *Dry Transfer of MoS_2 Flakes.* Few-layer MoS_2 devices were prepared by the commonly used pickup and dry transfer methods.[35,36] MoS_2 was mechanically exfoliated to obtain few-layer isolated flakes from commercially available bulk MoS_2 crystals on precleaned (i.e., Piranha solution, oxygen plasma, and solvent) substrates. A polydimethylsiloxane (PDMS) sheet was cut into small pieces and placed on a precleaned glass slide with double-sided tape. A 6% solution of polypropylene carbonate (PPC, Sigma-Aldrich) in chloroform was then spin coated on the glass/tape/PDMS stack. This transfer slide was loaded into the probe arm of the transfer setup and brought into contact with the desired flake at room temperature. The stage was heated to 90 °C and maintained at that temperature for 1 min. After the temperature of the stage was returned to room temperature, by natural or forced cooling, the transfer slide was slowly disengaged. The picked-up flake was transferred to the prepatterned via holes and heated

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to 155 °C to release the polymer. The polymer was dissolved in chloroform, and the structure was cleaned with solvent and annealed (200 sccm Ar/200 sccm H_2) at 360 °C for 3 h.

Phase Transformation of MoS_2. To achieve phase transformation in MoS_2, we used a common chemical method[20,37] involving exposure of 2H-MoS_2 to *n*BuLi solution, which is a strong reducing agent. 2H-MoS_2 samples were immersed in 2 M *n*BuLi (10 mL, Sigma-Aldrich) in a N_2-filled glovebox and then rinsed thoroughly with hexane. Li atoms can be inserted into MoS_2 layers to form Li_xMoS_2, the hydration of which results in MoS_2 and LiOH.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.6b03999.

Additional data concerning CVD growth and Raman characterization of MoS_2, device fabrication, block copolymer self-assembly; details of MVS, NEGF, and DFT calculations (PDF)

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Author Contributions

A.N. conceived the device, coordinated the study, and performed the device measurements. A.Z. fabricated the MoS_2 devices, performed the optical characterizations, and contributed to the device measurements. R.N.S. designed the device modeling approach and performed the modeling. A.T.K.G. developed the DSA-BCP technique and applied it to the MoS_2 devices. X.L. grew CVD MoS_2. W.C. and S.F. performed the DFT calculations. M.S.D., J.K., E.K., K.K.B., D.A., and T.P. supervised the research and provided scientific support. All authors contributed to the writing of the manuscript.

Notes

The authors declare no competing financial interest.

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