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A Dynamically Reconfigurable Ambipolar Black Phosphorus Memory Device

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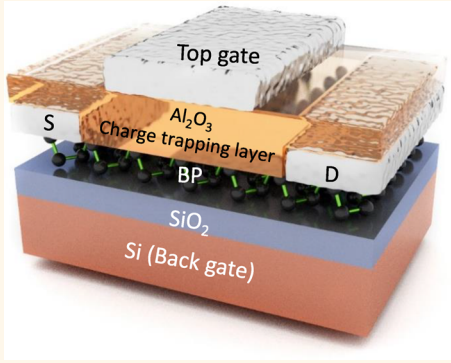
Supporting Information

ABSTRACT: **Nonvolatile charge-trap memory plays an important role in many modern electronics technologies, from portable electronic systems to large-scale data centers. Conventional charge-trap memory devices typically work with fixed channel carrier polarity and device characteristics. However, many emerging applications in reconfigurable electronics and neuromorphic computing require dynamically tunable properties in their electronic device components that can lead to enhanced circuit versatility and system functionalities. Here, we demonstrate an ambipolar black phosphorus (BP) charge-trap memory device with dynamically reconfigurable and polarity-reversible memory behavior. This BP memory device shows versatile memory properties subject to electrostatic bias. Not only the programmed/erased state current ratio can be continuously tuned by the back-gate bias, but also the polarity of the carriers in the BP channel can be reversibly switched between electron- and hole-dominated conductions, resulting in the erased and programmed states exhibiting interchangeable high and low current levels. The BP memory also shows four different memory states and, hence, 2-bit per cell data storage for both n-type and p-type channel conductions, demonstrating the multilevel cell storage capability in a layered material based memory device. The BP memory device with a high mobility and tunable programmed/erased state current ratio and highly reconfigurable device characteristics can offer adaptable memory device properties for many emerging applications in electronics technology, such as neuromorphic computing, data-adaptive energy efficient memory, and dynamically reconfigurable digital circuits.**



KEYWORDS: *two-dimensional materials, black phosphorus, nonvolatile memory, reconfigurable, multilevel-cell*

Recently, the growing importance of reconfigurable electronic systems[1,2] and a wide range of bioinspired electronic applications promoted intense research in developing electronic devices with dynamically reconfigurable properties.[3−7] Unlike conventional electronic devices that operate with fixed characteristics, these emerging applications often demand devices with tunable characteristics and reconfigurable functionalities.[3,4,7−11] Most of the research activities in this field so far have been focused on developing logic switches with reconfigurable behaviors,[3,12−14] while it is also highly desired to develop memory devices with dynamic tunability in their key performance parameters such as the channel carrier polarity and the programmed/erased state current ratios. Nonvolatile (NV) charge-trap memory is a popular type of solid-state memory technology[15−17] due to its excellent data storage performance and device scalability. The typical programming operation is based on the charge storage in the gate dielectric, leading to a shift in the threshold voltage of its field-effect current modulation behavior. Black phosphorus (BP) has recently emerged as a layered thin-film material with a moderate bandgap of 0.3 eV. Its comparable electron and hole carrier effective masses have resulted in

Received: September 17, 2016
Accepted: October 29, 2016
Published: October 29, 2016

DOI: 10.1021/acsnano.6b06293
ACS Nano 2016, 10, 10428−10435

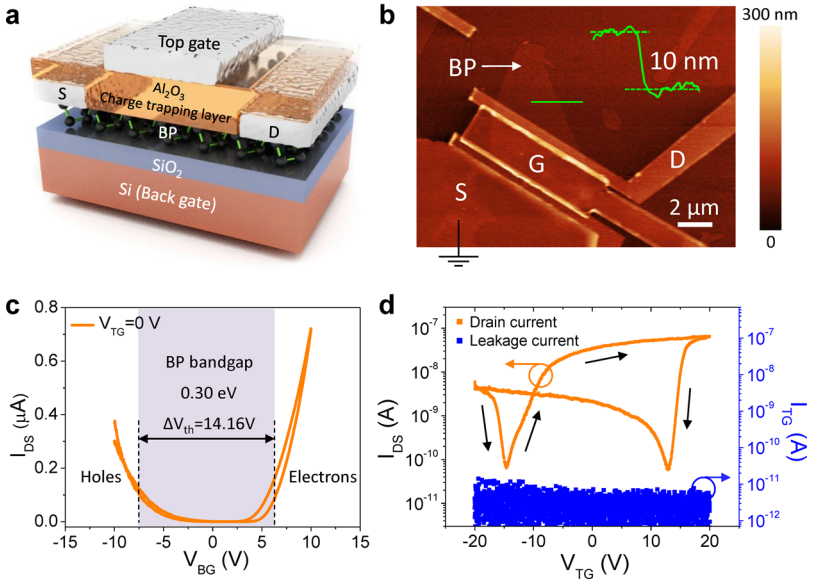


Figure 1. Device structure, fabrication, and I–V characteristics. (a) Schematic of the ambipolar BP charge-trap memory device. The 30 nm Al_2O_3 acts as the charge-trapping layer. (b) AFM image of the sample. The thickness of the BP flake is ~10 nm. (c) Ambipolar conduction in the as-fabricated BP FET subject to back-gate bias, indicating its 0.3 eV bandgap. (d) Typical hysteresis window of the BP charge-trap memory by top-gate control under zero back-gate voltage. The leakage current is well below 20 pA under all of the bias conditions shown in the plot.

balanced electron and hole mobility, and both can be above 1000 $cm^2/(V\ s)$ at room temperature.[18] Field-effect transistors (FET) with BP as the channel material has also shown a respectable on/off current ratio exceeding 10^5.[5,19−22] These properties made BP attractive for charge-trap memory device applications, while its relatively small bandgap can enable significant modification of the carrier density and even ambipolar conductions in the channel by electrostatic bias, offering opportunities for developing charge-trap memory devices with highly reconfigurable characteristics that are hard to achieve using conventional semiconductors, as well as in other layered 2D materials such as MoS_2 and graphene. MoS_2-based charge-trap memory devices typically have limited tunability[23,24] in its characteristics due to its relatively large bandgap above 1.8 eV. On the other hand, the graphene-based devices[25−28] have low programmed/erased state current ratios due to its zero bandgap.

In this work, a BP-based ambipolar memory device with dynamically reconfigurable memory behavior is reported. The key feature of the device is that the channel polarity can be dynamically tuned such that the programmed and erased state current levels can be reversibly changed by electrostatic bias, which can, for example, enable dynamic reconfigurability between active-high and active-low logic[29,30] in the memory data output. BP with a moderate 0.3 eV bandgap and ambipolar transport is ideally suited for such applications. Furthermore, the devices show a respectable memory window and tunable programmed/erased state current ratios as well as demonstrate 2-bit per cell data storage in 2D material based memory devices.

RESULTS AND DISCUSSION

Figure 1a shows the structure of the reconfigurable BP charge-trap memory device. This device employs BP as the channel material, which can provide ambipolar hole and electron conductions in the channel under different back-gate voltages. Here, the back-gate terminal is used to provide electrostatic bias that can allow for the modulation of the Fermi level and carrier density in the BP channel. BP flakes were first exfoliated on SiO_2 (90 nm)/Si substrate. A previous empirical study has shown that 5−10 nm thick BP sample can give the best trade-off between carrier mobility and device on/off current ratio.[19] As a result, BP flakes with a thickness of 5−10 nm are typically selected as the channel material followed by e-beam lithography and metal deposition, Cr/Au (3 nm/40 nm), to form the source and drain electrodes. In order to realize ambipolar characteristics in BP transistors, Cr/Au can typically be selected as the contact metal to enable the ambipolar conduction[19] since the work function of Cr (4.5 eV) is close to the midgap of BP.[31] A 30 nm Al_2O_3 layer is then deposited using atomic layer deposition (ALD) as the gate dielectric of the device to function as both the charge-trapping and charge-blocking layer. Finally, the top gate (control gate) electrode Cr/Au (3 nm/40 nm) is fabricated. Figure 1b shows the atomic force microscopy (AFM) image of the as-fabricated device. The inset shows the thickness of this particular BP flake. The fabricated BP memory device can operate with either electron or hole dominated conductions in the channel depending on the back-gate bias (Figure 1c). This is enabled by the ambipolar nature of the BP channel, which is a result of the relatively small bandgap of this material, and the metal contacts used that allows both electron and hole injection into the channel. A positive V_{BG} can tune the BP Fermi level close to the conduction band edge (n-type), while the Fermi level can be tuned close to the valence band edge (p-type) at negative V_{BG} bias. As a result, the device is in the OFF state for V_{BG} ranging from −7.92 to +6.24 V. The bandgap of BP can be estimated by the following formula[8]

$$E_g = q\Delta V_{th} \Big/ \left[\frac{SS_n + SS_p}{2} \Big/ SS_{60}\right] \quad (1)$$

where q is the electron charge, ΔV_{th} is the difference in the threshold voltages for the electron and hole branches, and SS_n and SS_p are the subthreshold slopes for the electron and hole

DOI: 10.1021/acsnano.6b06293
ACS Nano 2016, 10, 10428−10435

conducting branches, respectively. The extracted values of SS_n and SS_p are 1.98 and 3.59 V/dec for this device. SS_{60} is the thermodynamically limited subthreshold slope (60 mV/dec) at room temperature. By extracting the parameters from Figure 1c, the bandgap is estimated to be ∼0.30 eV, which agrees with the 0.3 eV bandgap of BP reported in theoretical studies and other experimental work in the literature.[32−34] The transfer curve of a BP device with back-gate modulation is shown in Figure S1 of the Supporting Information. The minimum conductivity point is located close to 0 V bias (at ∼1.2 V for a 90 nm SiO_2 gate oxide), and the electron and hole conduction branches are fairly symmetrical, indicating that the BP material is relatively intrinsic.

Figure 1d shows the transfer curve of the BP memory device for both forward and backward top-gate voltage sweeps at V_{BG} = 0 V. There are two hysteresis windows, which indicate the ambipolar transport of the device. Moreover, the positive shift of the minimum conductivity point during the forward/backward sweeps of the gate voltage is a signature of the charge transfer effect[35] between the BP and Al_2O_3. The memory window, i.e., the shift of the threshold voltage, in the n-type channel conduction branch, can be as large as 16.2 V. For both p-type (at negative V_{BG}) and n-type (at positive V_{BG}) conductions in the BP channel, a positive voltage applied to the top gate (control gate) always shifts the threshold voltage of the transfer curve more positive (or less negative). The threshold voltage shift indicates that a transfer of charge has occurred under the application of the gate voltage. This transfer of charge could be either due to the movement of the local charges already present in the system, e.g., electrons or ions in the Al_2O_3 dielectric or by the injection or removal of electrons from the dielectric through the electrodes or BP channel. The "sign" of the threshold voltage shift indicates that negative charges have been injected into the Al_2O_3 dielectric (the sign of the threshold voltage shift will be opposite if the charge reconfiguration is due to mobile ions or electrons in the dielectric). Hence, we can use a positive voltage at the control gate to program the BP memory device for both p-type and n-type channel conduction by injecting electrons into the Al_2O_3 charge-trapping layer. At a typical programming voltage of 20 V, the vertical electric field at the programming voltage is estimated to be ∼6.7 MV/cm at the BP/Al_2O_3 interface based on the parallel plate model. Since this is close to the typical breakdown field 5−10 MV/cm[36] of Al_2O_3, it is reasonable to expect that charges can be trapped deep inside the Al_2O_3. Under these high fields, electrons are easily injected into the dielectric and remain trapped in the metastable states. The observed device behavior also agrees with that in carbon nanotube[37−40] and organic[41−43] semiconductor based non-volatile memory devices operating with a dielectric charge-trap mechanism.[24,25]

As shown in Figure 2a, for hole conduction in the BP channel at negative V_{BG}, the stored electrons cause a positive shift in the threshold voltage for the p-type channel, resulting in a higher current level (Figure 2c) in the programmed state compared to the erased state at a given read voltage. For n-type conduction in the BP channel at positive V_{BG} bias (Figure 2b), the stored negative charges also cause a positive shift in the threshold voltage. Due to n-type channel conduction in BP, this positive V_T shift would result in a lower current level (Figure 2d) in the programmed state compared to the erased state at a given read voltage. Hence, as shown in Figure 2, by tuning the polarity and the amplitude of the back-gate bias, a

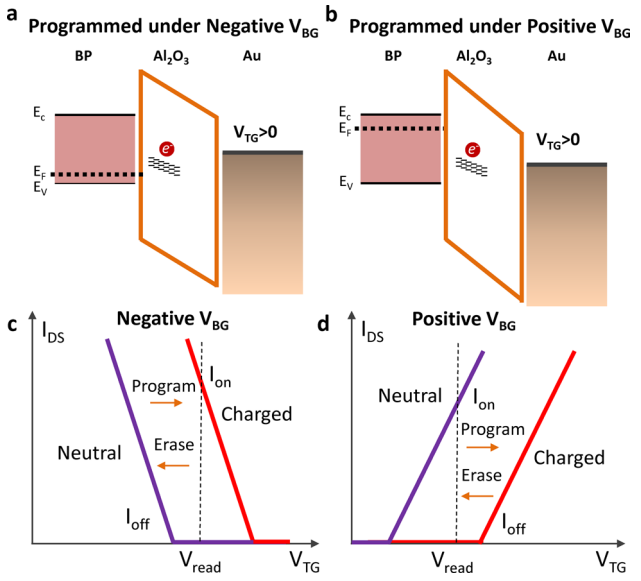


Figure 2. Operation mechanism of the BP reconfigurable charge-trap memory device. (a) Energy diagram for the programming process at negative back-gate bias. The channel conduction is p-type. (b) Energy diagram for the programming process at positive back-gate bias. The channel conduction is n-type. For both (a) and (b), a positive voltage pulse on the top (control) gate allows the electrons to be injected into the Al_2O_3 layer, shifting the threshold voltage more positive. (c) I_{DS}−V_{TG} characteristics at positive back-gate bias with (charged) and without charges (neutral) trapped in the Al_2O_3 layer, respectively. In this case, the programming operation shifts the threshold voltage more positive (or less negative). The read current level is higher for the programmed state and lower for the erased state. (d) The I_{DS}−V_{TG} characteristics under negative back-gate bias with (charged) and without charges (neutral) trapped in the Al_2O_3 layer, respectively. In this case, the programming operation also shifts the threshold voltage more positive (or less negative). The read current level is lower for the programmed state and higher for the erased state.

reconfigurable charge-trap memory can be realized. Parts a and b of Figure 3 show the I−V characteristics of the fabricated BP memory devices at V_{BG} = −20 and +20 V, respectively. The top-gate (control gate) bias was swept from $-V_{TG,max}$ to $+V_{TG,max}$ followed by $+V_{TG,max}$ to $-V_{TG,max}$, respectively. The control gate threshold voltage shift ΔV_{th} increases with higher $V_{TG,max}$, indicating that a larger programming voltage on the top gate can lead to a larger amount of charges being injected into the dielectric layer. As shown in Figure 3c,d, ΔV_{th} increases fairly linearly with $V_{TG,max}$ for both p-type and n-type conduction branches at V_{BG} = −20 and +20 V, respectively, demonstrating that the amount of charge carriers injected into the Al_2O_3 layer can be well-controlled by tuning the programming voltage at the top gate. This allows the realization of ambipolar multibit data storage in a single BP memory device. The reconfigurable hysteresis curves and the associated memory effects have been demonstrated in more than 10 ambipolar BP memory devices (see Figure S2 of the Supporting Information).

The multilevel cell data storage capability is experimentally demonstrated by applying program/erase pulses to the device and monitor the drain current up to 1200 s under a 100 mV source-drain bias with the read voltage chosen at V_{TG}= 0 V. As shown in Figure 4a, for p-type BP channel conduction at V_{BG} = −20 V, the initial current levels are 0.2, 1.5, and 4.3 μA after the

DOI: 10.1021/acsnano.6b06293
ACS Nano 2016, 10, 10428−10435

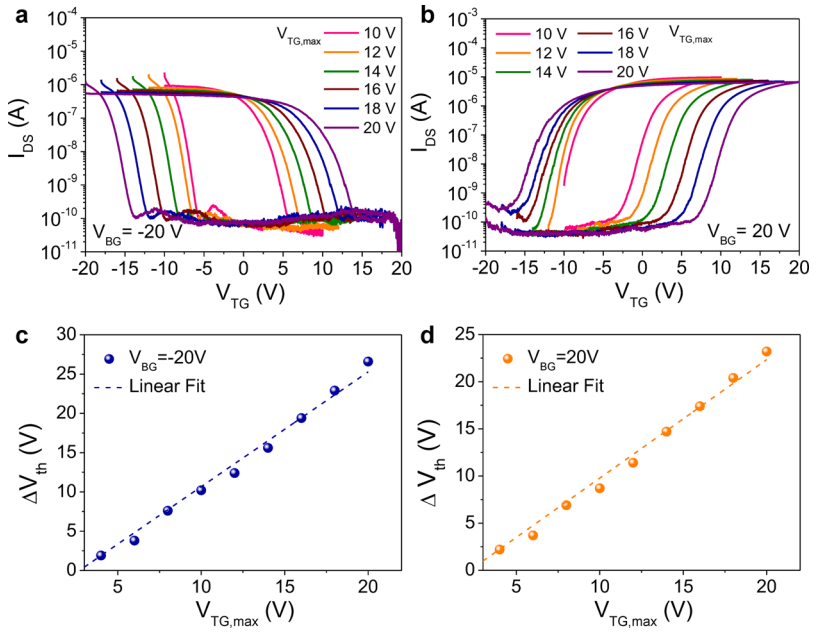


Figure 3. Tunable ambipolar BP memory device characteristics. I_{DS} vs V_{TG} characteristics for (a) V_{BG} = −20 V and (b) V_{BG} = 20 V at different $V_{TG,max}$ for a 5 nm thick BP channel device with V_{DS} = 100 mV. The dependence of the shift in the threshold voltage ΔV_{th} on $V_{TG,max}$ under (c) V_{BG} = −20 V and (d) V_{BG} = 20 V, respectively.

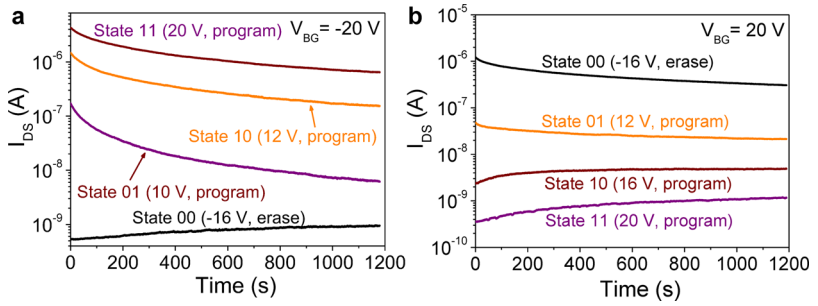


Figure 4. Multilevel-cell storage. I_{DS} vs time characteristics at (a) V_{BG} = −20 V for the erased and programmed states (00, 01, 10, and 11) of the device with 10 V, 12, and 20 V programming pulses (100 ms duration) and at (b) V_{BG} = 20 V for the erased and programmed states (00, 01, 10, and 11) of the device with 12, 16, and 20 V programming pulses (100 ms duration).

device is programmed at V_{TG} = 10, 12, and 20 V pulses, respectively. The data integrity is not compromised after 1200 s and at a programmed/erased state current ratio above 10^3. It can be expected based on the extrapolation from the measured data that the retention time of these memory devices can be several orders of magnitude beyond the measured value (see Figure S3 of the Supporting Information). By controlling the program voltage at the top gate, the amount of electrons injected into the Al_2O_3 dielectric can be controlled. Here, by programming the device at V_{TG} = 10, 12, and 20 V, the device shows four different current levels including the −16 V erased state. The four different states can be denoted as 00, 01, 10, and 11 states corresponding to the −16 V erased state and the 10, 12, and 20 V programmed states. A similar 2-bit per cell data storage capability is also demonstrated for the n-type channel conduction at V_{BG} = 20 V as shown in Figure 4b. The injection of electrons into the Al_2O_3 dielectric will shift the threshold voltage more positive for both the n-type and p-type channel operations. It will lead to higher read current in the programmed state than the erased state for the p-type conduction regime, but for the n-type conduction regime of this ambipolar BP memory device, the positive shift in the threshold voltage will lead to a reduced read current in the programmed state compared to the erased state as illustrated in Figure 2d. This is evident in Figure 4b, which shows that for n-type channel conduction the read current is 1.2 μA at the erased state and the read currents switch to lower levels for the three programmed states. The programmed state read currents for programming at 12, 16, and 20 V are 48.2, 2.3, and 0.4 nA, respectively. The initial change in the current level as shown in Figure 4 can be due to the possible presence of PO_x at the BP/Al_2O_3 interface (see detailed discussion in the Supporting Information). The charges injected into PO_x can escape much easier than the charges trapped in Al_2O_3. Although precautions have be taken to prevent the oxidation of the BP sample by processing the device in an Ar glovebox as much as possible, it is still possible that small traces of PO_x could form during the device fabrication process.

Because of the screening effect, the ability of the gate electric field to modulate charges in the BP channel becomes weaker as the BP channel thickness increases. This has a profound impact on the device characteristics. Parts a and b of Figure 5 summarize the programmed (11 state) and erased (00 state) state current levels and the programmed/erased state current

DOI: 10.1021/acsnano.6b06293
ACS Nano 2016, 10, 10428−10435

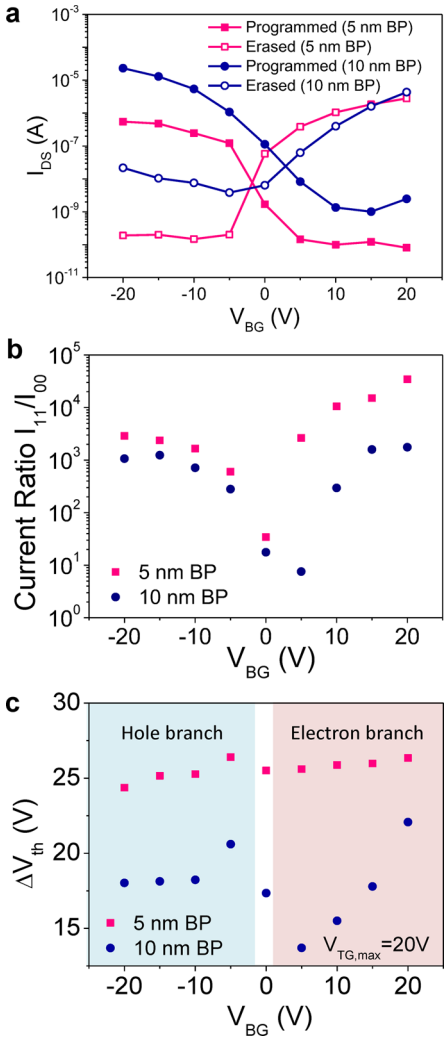


Figure 5. Thickness dependence of the device characteristics. (a) Programmed and erased state currents as a function of the back-gate bias for both the 5 and 10 nm thick BP channel devices. (b) Programmed/erased states current ratio as a function of the back-gate bias for the 5 and 10 nm devices. (c) Shift in the threshold voltage for the 5 and 10 nm samples at different back-gate bias for $V_{TG,max}$ = 20 V. Both devices are identical in their structures and operating conditions except for the channel thickness.

ratio I_{11}/I_{00} at different biases of V_{BG} for two BP memory devices with the BP layer thicknesses of 5 and 10 nm, respectively. For V_{BG} significantly lower than 0 V, the programmed state current is higher than the erased state current, while for V_{BG} significantly higher than 0 V, the programmed state current is lower than the erased state current. A clear transition around V_{BG} = 0 V is observed for both the 5 and 10 nm BP devices. Furthermore, there is a clear change in the programmed/erased state current ratio due to the modulation of the BP channel Fermi level by the back gate bias from the valence band edge to the midgap and then to the conduction band edge. For V_{BG} = 0 V, the trapped charges in the Al_2O_3 dielectric shift the Fermi level in the BP layer around its midgap, and the change in the channel current is less significant. The current level change is more significant when the Fermi level in the BP layer is closer to the bandgap edges for larger positive and negative biases of V_{BG}. For the 10 nm BP device, the programmed/erased state current ratio I_{11}/I_{00} is around 10 at V_{BG} = 0 V. At larger negative or positive V_{BG} biases, this ratio can be enhanced to over 10^3. Hence, in these BP memory devices, not only can the channel polarity, and thus the programmed and erased state current levels, be reversibly tuned but also the programmed/erased state current ratio can be dynamically controlled by the back-gate bias. Moreover, the 5 nm thick BP channel device has a larger I_{11}/I_{00} ratio compared to the 10 nm thick BP channel device. This ratio is close to 40 at zero back-gate bias and increases to over 4×10^4 at V_{BG} = 20 V. Furthermore, as shown in Figure 5c, the device with 5 nm thick channel also has a larger memory window compared to the device with 10 nm thick channel for the same operating conditions. This reflects the reduced screening effect[19] in thinner BP samples and hence more significant carrier modulation in the channel.

To further demonstrate the reconfigurable behavior of the ambipolar BP memory device, its dynamic characteristics are studied. The repeated switching between the programmed and erased states for both p-type and n-type channel conductions is shown as a function of time in Figure 6a,b. In each program/erase cycle, a positive pulse (20 V, 100 ms) is applied to the top gate for programming the device followed by a negative pulse (−20 V, 100 ms) to erase the stored data. As shown in Figure 6a,b, for p-type conduction in the channel at V_{BG} = −20 V, the programming voltage pulse switches the channel current level measured at V_{read} = 0 V from low to high, and for n-type conduction in the channel at V_{BG} = 20 V the program voltage pulse switches the channel current level from high to low. A negative erase pulse applied at the top gate can remove the trapped charges from Al_2O_3, and the read current level can recover to the erased state for both p-type and n-type channel conduction operations, respectively. The dependence of the memory properties on the programming pulse width is shown in Figure S4 of the Supporting Information. The calculated trapping rate is in the range of 10^{15}–10^{12} cm^{-2} s^{-1}. The endurance of the device is also studied by applying +20 and −20 V pulses with 100 ms duration. The results in Figure 6c,d indicate the repeatable and stable cycling in 100 cycles between the programmed and erased states for V_{BG} = −20 and +20 V. Moreover, there is no significant performance degradation for the device over at least 2 months due to the well-protected BP channel by Al_2O_3 encapsulation. A detailed study on protecting BP using Al_2O_3 has also been reported in ref 44, which used near-field optical measurement and atomic force microscopy measurement to show that BP protected by >10 nm of Al_2O_3 shows no degradation after more than 2 months. The dynamic characteristics of the device at different back-gate bias V_{BG} are also measured. Figure 6e shows the read current of the device measured with respect to time for repeated cycles of program and erase operations. The colors in the plot correspond to data points measured at different values of V_{BG} bias. As the back-gate bias increases from −20 to 0 V, the BP channel has p-type conduction. The high and low current levels represent the programmed and erased states, respectively. In addition, the programmed/erased states current ratio decreases with increasing back-gate bias and the BP channel is relatively intrinsic around V_{BG} = 0 V. As the back-gate voltage increases from 0 to 20 V, the channel conduction becomes n-type, and it is clear that the programmed state now has a lower current level compared to the erased state due to the reversal of the channel polarity, demonstrating the ambipolar reconfigurability in the BP memory device. The programmed/erased states current ratio also increases at a more positive V_{BG} bias. One direct

DOI: 10.1021/acsnano.6b06293
ACS Nano 2016, 10, 10428−10435

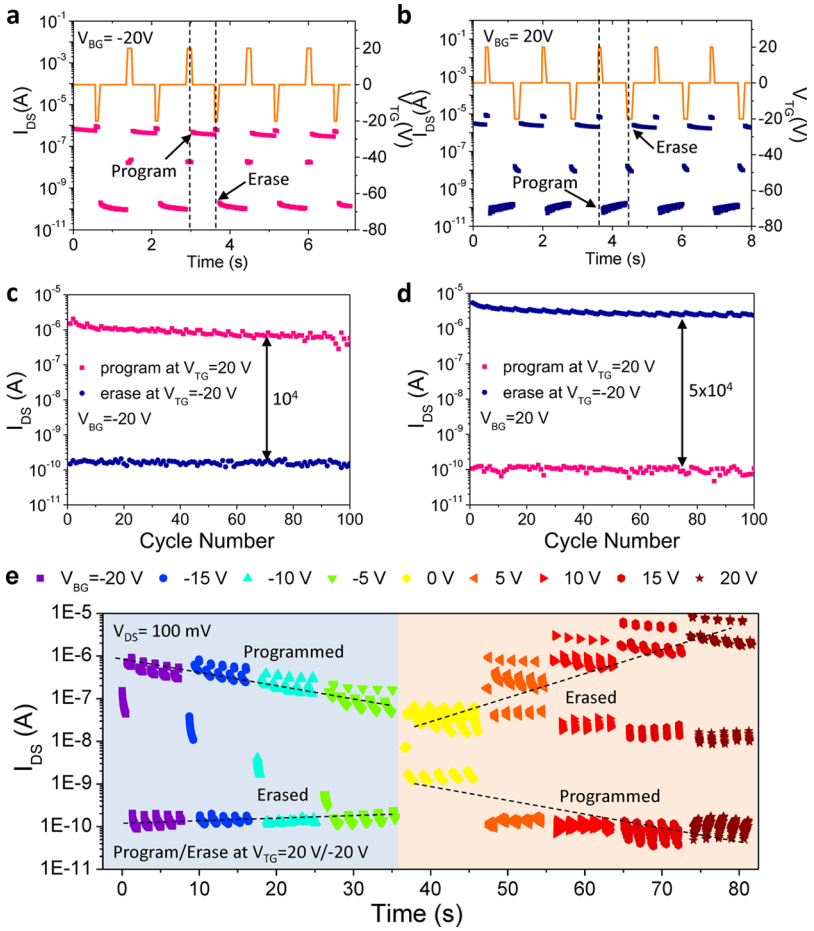


Figure 6. Dynamically tunable program/erase operations. (a) Dynamic switching between the erased state (low current, device off) and the programmed state (high current, device on) at V_{BG} = −20 V for the 5 nm thick BP channel device. (b) Dynamic switching between the erased state (high current, device on) and the programmed state (low current, device off) at V_{BG} = 20 V for the same device. (c) Performance of the 5 nm thick BP channel device for 100 cycles of program/erase operations at V_{BG} = −20 V. (d) Performance of the 5 nm thick BP channel memory device for 100 cycles of program/erase operations at V_{BG} = 20 V. The program and erase pulses are +20 V, 100 ms and −20 V, 100 ms, respectively. The program and erase pulses are +20 V, 100 ms and −20 V, 100 ms, respectively, for (c) and (d). (e) Dynamically tunable memory characteristics of the ambipolar BP memory device. The 5 nm thick BP channel memory device is biased at different back-gate voltages. The device is programmed and erased at 20 V and −20 V, respectively. The programmed/erased state current ratio and the polarity of the channel conduction can both be dynamically and reversibly tuned. The channel conduction is p-type for negative V_{BG} and n-type for positive V_{BG}.

application of this reconfigurable device, for example, is that the output data read from the memory device can be dynamically switched between active-high and active-low logic[45] implementations that can be useful for many reconfigurable electronic systems. It is also attractive for the emerging field of neuromorphic computations where many biomimetic applications demand device reconfigurability and diverse functionalities, for example, as an artificial synaptic device that can dynamically reconfigure between excitatory and inhibitory responses.[7]

CONCLUSIONS

In summary, an ambipolar multilevel-cell black phosphorus nonvolatile charge-trap memory is demonstrated that shows dynamically reconfigurable characteristics. The channel polarity can be reversibly switched between electron and hole conductions. Not only can the programmed/erased state current levels be widely tuned by electrostatic bias, but also their high and low levels can be completely reversed due to the ambipolar conduction in the narrow 0.3 eV bandgap black phosphorus channel. The BP memory also shows a programmed/erased state current ratio up to 5 × 10^4 with multilevel cell data storage capabilities. Such reconfigurable BP memory can find many applications in the dynamically reconfigurable active-high/active-low logic, data-adaptive energy efficient memory, and also the emerging field of neuromorphic computations[46] as artificial synaptic devices that can dynamically reconfigure[7] between excitatory and inhibitory responses.

METHODS

Device Fabrication. The fabrication of the devices started with the mechanical exfoliation of BP thin films from bulk crystals (Smart Element) onto 90 nm SiO_2 on a silicon substrate in an argon-filled glovebox (Mbraun, Inc.) with both oxygen and water concentrations well below one part per million (1 ppm). The sample electrode pattern was then created using a Vistec EBPG 5000+ 100 kV electron-beam lithography system with PMMA A4 resist spin-coated at 3000 rpm for 1 min. Cr/Au (5/30 nm) were then deposited, followed by a lift-off process in acetone to form the source and drain electrodes. The total accumulated time of BP exposure to air before ALD is less than 15

DOI: 10.1021/acsnano.6b06293
ACS Nano 2016, 10, 10428−10435

min. The 30 nm thick Al_2O_3 top-gate dielectric was formed by ALD using a Cambridge NanoTech Savannah system. Cr/Au (5/30 nm) top-gate electrodes were fabricated using the same metallization procedure as discussed above.

AFM Measurements. The AFM images were captured using a Bruker Dimension-Icon FastScan system.

Electrical Measurements. The electrical characterizations were carried out using an Agilent B1500A parameter analyzer in a Lakeshore cryogenic probe station. The measurements are performed in vacuum ($<1 \times 10^{-4}$ Torr) at room temperature. All of the measurements of the transfer curves used the same sweeping rate of 0.68 V/s. The pulse is generated under *I*−*V* list sweep mode with a minimum pulse width of 10 ms. Additional pulse measurements were performed using a Keithley 4200 system with the pulse measurement module.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.6b06293.

Figures S1−S4 and additional references (PDF)

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Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work is supported by the Army Research Office, Grant No. W911NF-16-1-0435, and the Northrop Grumman Institute of Optical Nanomaterials and Nanophotonics (NG-ION^2) at USC. F.X. acknowledges support from the Office of Naval Research through the Young Investigator Program (Grant No. N00014-15-1-2733) and the Air Force Office of Scientific Research (Grant No. FA9550-14-1-0277). Q.X. thanks the Air Force Office for Scientific Research for support (Grant No. FA9550-12-1-0038).

REFERENCES

(1) Wong, H.-S. P.; Salahuddin, S. Memory Leads the Way to Better Computing. *Nat. Nanotechnol.* **2015**, *10*, 191−194.

(2) Qian, C.; Huang, L.; Xie, P.; Xiao, N.; Wang, Z. A Study on Non-volatile 3D Stacked Memory for Big Data Applications. In *Algorithms and Architectures for Parallel Processing*; Springer, 2015; pp 103−118.

(3) Joo, S.; Kim, T.; Shin, S. H.; Lim, J. Y.; Hong, J.; Song, J. D.; Chang, J.; Lee, H.-W.; Rhie, K.; Han, S. H. Magnetic-Field-Controlled Reconfigurable Semiconductor Logic. *Nature* **2013**, *494*, 72−76.

(4) Kim, W. Y.; Kim, H.-D.; Kim, T.-T.; Park, H.-S.; Lee, K.; Choi, H. J.; Lee, S. H.; Son, J.; Park, N.; Min, B. Graphene-Ferroelectric Metadevices for Nonvolatile Memory and Reconfigurable Logic-Gate Operations. *Nat. Commun.* **2016**, *7*, 10429.

(5) Luo, Z.; Zhang, X.; Xiong, C.; Chen, J. Silicon-Based Current-Controlled Reconfigurable Magnetoresistance Logic Combined with Non-Volatile Memory. *Adv. Funct. Mater.* **2015**, *25*, 158−166.

(6) Kuzum, D.; Yu, S.; Wong, H. P. Synaptic Electronics: Materials, Devices and Applications. *Nanotechnology* **2013**, *24*, 382001.

(7) Tian, H.; Mi, W.; Wang, X.-F.; Zhao, H.; Xie, Q.-Y.; Li, C.; Li, Y.-X.; Yang, Y.; Ren, T.-L. Graphene Dynamic Synapse with Modulatable Plasticity. *Nano Lett.* **2015**, *15*, 8013−8019.

(8) Xu, H.; Fathipour, S.; Kinder, E. W.; Seabaugh, A. C.; Fullerton-Shirey, S. K. Reconfigurable Ion Gating of 2H-$MoTe_2$ Field-Effect Transistors Using Poly (ethylene oxide)-$CsClO_4$ Solid Polymer Electrolyte. *ACS Nano* **2015**, *9*, 4900−4910.

(9) Tian, H.; Zhao, H.; Wang, X. F.; Xie, Q. Y.; Chen, H. Y.; Mohammad, M. A.; Li, C.; Mi, W. T.; Bie, Z.; Yeh, C. H. *In Situ* Tuning of Switching Window in A Gate-Controlled Bilayer Graphene-Electrode Resistive Memory Device. *Adv. Mater.* **2015**, *27*, 7767−7774.

(10) Sangwan, V. K.; Jariwala, D.; Kim, I. S.; Chen, K.-S.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C. Gate-Tunable Memristive Phenomena Mediated by Grain Boundaries in Single-Layer MoS_2. *Nat. Nanotechnol.* **2015**, *10*, 403−406.

(11) Bessonov, A. A.; Kirikova, M. N.; Petukhov, D. I.; Allen, M.; Ryhänen, T.; Bailey, M. J. Layered Memristive and Memcapacitive Switches for Printable Electronics. *Nat. Mater.* **2014**, *14*, 199−204.

(12) Gokhale, M.; Graham, P. S. Reconfigurable Logic Devices. In *Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays*; Springer, 2005; pp 11−36.

(13) Berrettini, G.; Simi, A.; Malacarne, A.; Bogoni, A.; Poti, L. Ultrafast Integrable and Reconfigurable XNOR, AND, NOR, and NOT Photonic Logic Gate. *IEEE Photonics Technol. Lett.* **2006**, *18*, 917−919.

(14) Fawcett, B. K. Taking Advantage of Reconfigurable Logic. *Proc. Annu. IEEE Int. ASIC Conf.* **1994**, 227−230.

(15) Pavan, P.; Bez, R.; Olivo, P.; Zanoni, E. Flash Memory Cells-An Overview. *Proc. IEEE* **1997**, *85*, 1248−1271.

(16) Lai, S. K. Flash Memories: Successes and Challenges. *IBM J. Res. Dev.* **2008**, *52*, 529−535.

(17) Bez, R.; Camerlenghi, E.; Modelli, A.; Visconti, A. Introduction to Flash Memory. *Proc. IEEE* **2003**, *91*, 489−502.

(18) Chen, X.; Wu, Y.; Wu, Z.; Han, Y.; Xu, S.; Wang, L.; Ye, W.; Han, T.; He, Y.; Cai, Y. High-Quality Sandwiched Black Phosphorus Heterostructure and Its Quantum Oscillations. *Nat. Commun.* **2015**, *6*, 7315.

(19) Li, L.; Yu, Y.; Ye, G. J.; Ge, Q.; Ou, X.; Wu, H.; Feng, D.; Chen, X. H.; Zhang, Y. Black Phosphorus Field-Effect Transistors. *Nat. Nanotechnol.* **2014**, *9*, 372−377.

(20) Xia, F.; Wang, H.; Jia, Y. Rediscovering Black Phosphorus as an Anisotropic Layered Material for Optoelectronics and Electronics. *Nat. Commun.* **2014**, *5*, 4458.

(21) Liu, H.; Neal, A. T.; Zhu, Z.; Luo, Z.; Xu, X.; Tománek, D.; Ye, P. D. Phosphorene: An Unexplored 2D Semiconductor with A High Hole Mobility. *ACS Nano* **2014**, *8*, 4033−4041.

(22) Koenig, S. P.; Doganov, R. A.; Schmidt, H.; Neto, A. C.; Oezyilmaz, B. Electric Field Effect in Ultrathin Black Phosphorus. *Appl. Phys. Lett.* **2014**, *104*, 103106.

(23) Zhang, E.; Wang, W.; Zhang, C.; Jin, Y.; Zhu, G.; Sun, Q.; Zhang, D. W.; Zhou, P.; Xiu, F. Tunable Charge-Trap Memory Based on Few-Layer MoS_2. *ACS Nano* **2015**, *9*, 612−619.

(24) Bertolazzi, S.; Krasnozhon, D.; Kis, A. Nonvolatile Memory Cells Based on MoS_2/Graphene Heterostructures. *ACS Nano* **2013**, *7*, 3246−3252.

(25) Hong, A. J.; Song, E. B.; Yu, H. S.; Allen, M. J.; Kim, J.; Fowler, J. D.; Wassei, J. K.; Park, Y.; Wang, Y.; Zou, J. Graphene Flash Memory. *ACS Nano* **2011**, *5*, 7812−7817.

(26) Sup Choi, M.; Lee, G.-H.; Yu, Y.-J.; Lee, D.-Y.; Lee, S. H.; Kim, P.; Hone, J.; Yoo, W. J. Controlled Charge Trapping by Molybdenum Disulphide and Graphene in Ultrathin Heterostructured Memory Devices. *Nat. Commun.* **2013**, *4*, 1624.

(27) Imam, S.; Deshpande, T.; Guermoune, A.; Siaj, M.; Szkopek, T. Charge Transfer Hysteresis in Graphene Dual-Dielectric Memory Cell Structures. *Appl. Phys. Lett.* **2011**, *99*, 082109.

(28) Lee, S.; Song, E. B.; Kim, S.; Seo, D. H.; Seo, S.; Kang, T. W.; Wang, K. L. Impact of Gate Work-Function on Memory Characteristics in $Al_2O_3/HfO_x/Al_2O_3$/Graphene Charge-Trap Memory Devices. *Appl. Phys. Lett.* **2012**, *100*, 023109.

(29) Athas, W. C.; Svensson, L. J.; Koller, J. G.; Tzartzanis, N.; Chou, E. Y.-C. Low-Power Digital Systems Based on Adiabatic-Switching Principles. *IEEE Trans. VLSI Syst.* **1994**, *2*, 398−407.

(30) Bedeschi, F.; Bez, R.; Boffino, C.; Bonizzoni, E.; Buda, E.; Casagrande, G.; Costa, L.; Ferraro, M.; Gastaldi, R.; Khouri, O. 4-Mb

DOI: 10.1021/acsnano.6b06293
ACS Nano 2016, 10, 10428−10435

MOSFET-Selected Phase-Change Memory Experimental Chip. *IEEE Conf. Solid-State Circuits* **2004**, 207−210.
(31) Yan, R.; Fathipour, S.; Han, Y.; Song, B.; Xiao, S.; Li, M.; Ma, N.; Protasenko, V.; Muller, D. A.; Jena, D. Esaki Diodes in Van Der Waals Heterojunctions with Broken-Gap Energy Band Alignment. *Nano Lett.* **2015**, *15*, 5791−5798.
(32) Qiao, J.; Kong, X.; Hu, Z.-X.; Yang, F.; Ji, W. High-Mobility Transport Anisotropy and Linear Dichroism in Few-Layer Black Phosphorus. *Nat. Commun.* **2014**, *5*, 4475.
(33) Tran, V.; Soklaski, R.; Liang, Y.; Yang, L. Layer-Controlled Band Gap and Anisotropic Excitons in Few-Layer Black Phosphorus. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2014**, *89*, 235319.
(34) Morita, A. Semiconducting Black Phosphorus. *Appl. Phys. A: Solids Surf.* **1986**, *39*, 227−242.
(35) Wang, H.; Wu, Y.; Cong, C.; Shang, J.; Yu, T. Hysteresis of Electronic Transport in Graphene Transistors. *ACS Nano* **2010**, *4*, 7221−7228.
(36) Groner, M.; Elam, J.; Fabreguette, F.; George, S. M. Electrical Characterization of Thin Al_2O_3 Films Grown by Atomic Layer Deposition on Silicon and Various Metal Substrates. *Thin Solid Films* **2002**, *413*, 186−197.
(37) Fuhrer, M.; Kim, B.; Dürkop, T.; Brintlinger, T. High-Mobility Nanotube Transistor Memory. *Nano Lett.* **2002**, *2*, 755−759.
(38) Radosavljevic, M.; Freitag, M.; Thadani, K.; Johnson, A. Nonvolatile Molecular Memory Elements Based on Ambipolar Nanotube Field Effect Transistors. *Nano Lett.* **2002**, *2*, 761−764.
(39) Rinkiö, M.; Johansson, A.; Paraoanu, G.; Törmä, P. i. High-Speed Memory from Carbon Nanotube Field-Effect Transistors with High-K Gate Dielectric. *Nano Lett.* **2009**, *9*, 643−647.
(40) Li, G.; Li, Q.; Jin, Y.; Qian, Q.; Zhao, Y.; Xiao, X.; Wang, J.; Jiang, K.; Fan, S. Demonstration of Nonvolatile Multilevel Memory in Ambipolar Carbon Nanotube Thin-Film Transistors. *Appl. Phys. Express* **2015**, *8*, 065101.
(41) Chang, H. C.; Liu, C. L.; Chen, W. C. Flexible Nonvolatile Transistor Memory Devices Based on One-Dimensional Electrospun P3HT: Au Hybrid Nanofibers. *Adv. Funct. Mater.* **2013**, *23*, 4960−4968.
(42) Sekitani, T.; Yokota, T.; Zschieschang, U.; Klauk, H.; Bauer, S.; Takeuchi, K.; Takamiya, M.; Sakurai, T.; Someya, T. Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays. *Science* **2009**, *326*, 1516−1519.
(43) Narayanan Unni, K.; de Bettignies, R.; Dabos-Seignon, S.; Nunzi, J.-M. A Nonvolatile Memory Element Based on An Organic Field-Effect Transistor. *Appl. Phys. Lett.* **2004**, *85*, 1823.
(44) Gamage, S.; Li, Z.; Yakovlev, V. S.; Lewis, C.; Wang, H.; Cronin, S. B.; Abate, Y. Nanoscopy of Black Phosphorus Degradation. *Adv. Mater. Interfaces* **2016**, *3*, 1600121.
(45) Browne, M. C.; Clarke, E. M.; Dill, D. L.; Mishra, B. Automatic Verification of Sequential Circuits Using Temporal Logic. *IEEE Trans. Comput.* **1986**, *C-35*, 1035−1044.
(46) Indiveri, G.; Whatley, A. M.; Kramer, J. A Reconfigurable Neuromorphic VLSI Multi-Chip System Applied to Visual Motion Computation. *Proc. IEEE Int. Conf. Microelectron. Neural, Fuzzy and Bio-Inspired Syst.* **1999**, 37−44.

DOI: 10.1021/acsnano.6b06293
ACS Nano 2016, 10, 10428−10435